1969

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69-20,670

SIE, Charles Henry, 1934-
MEMORY CELL USING BISTABLE RESISTIVITY IN AMORPHOUS As-Te-Ge FILM.

Iowa State University, Ph.D., 1969
Engineering, electrical

University Microfilms, Inc., Ann Arbor, Michigan

MEMORY CELL USING BISTABLE RESISTIVITY IN AMORPHOUS As-Te-Ge FILM

by

Charles Henry Sie

A Dissertation Submitted to the
Graduate Faculty in Partial Fulfillment of
The Requirements for the Degree of
DOCTOR OF PHILOSOPHY

Major Subject: Electrical Engineering

Approved:

Signature was redacted for privacy.

In Charge of Major Work

Signature was redacted for privacy.

Head of Major Department

Signature was redacted for privacy.

Dean of Graduate College

Iowa State University
Ames, Iowa

1969

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I. INTRODUCTION

The primary goal of this thesis research is to establish the feasibility of using glass material with electrically reversible bulk bistable resistivity (abbreviated BSR) for digital memory application. The first part of this thesis describes the preparation of test devices using evaporated glass with bistable resistivity. As reported by others a glass composition of As-Te-Ge (1) was confirmed to exhibit BSR in bulk. The switchability of an evaporated As-Te-Ge film sandwiched between two orthogonal arrays of conductors then was ascertained. The second part of this thesis relates the measured device characteristics to memory array properties. The memory analysis indicates that it is necessary to place a non-linear element such as a diode in series with the BSR device in order to eliminate the array sneak path noises in a large memory array. The analysis shows that with suitable diodes electrically alterable read only memories can be achieved using BSR.

There are some inherent characteristics of BSR glass which make it attractive for digital memory applications. These characteristics are:

1. The phenomenon is non-volatile. Either high or low resistance states can be maintained without bias voltage or current.
2. Since this phenomenon seemed to be an alteration of the very local regions in the material, high memory cell densities appear achievable.
3. Batch fabrication process such as evaporation can be used in making the memory array.
4. The switching speed is in the fractional millisecond range.

BSR can best be characterized by its V-I curve as shown in Figure 1. The two stable resistance states are represented by the two slopes. Initially, the device is in its high resistance state, R_h. An external voltage is applied through a resistance, R_s. As the voltage across the device reached the threshold value, V_t, the device switched to its low resistance state, R_l, following the load line. It might well be pointed out that the intersection of the load line with R_l should be below the current threshold value, I_t when the voltage across the device reaches V_t. The device will remain in the low resistance state even if the external circuit is removed. In switching back from R_l to R_h, the value of R_s is decreased or a voltage source is used. When the current in the device reaches its threshold value, I_t, the device switches to its high resistance state. Here the intersection of R_s with R_h should be below V_t, when the current in the device is I_t. Typical values of R_h and R_l are 10^6 ohms and 10^2 ohms respectively. The R_h value varies inversely with the cross sectional area.

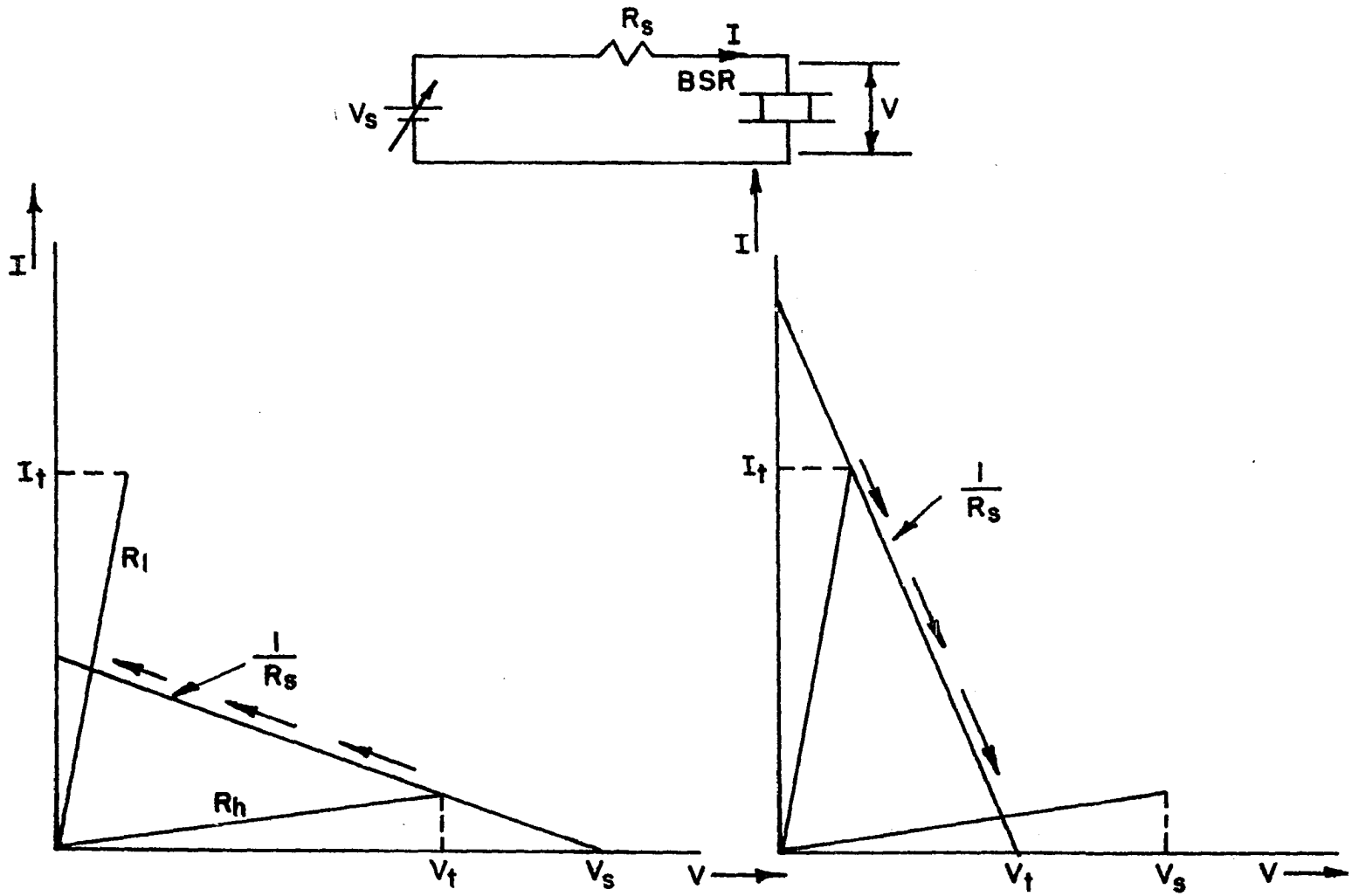

FIGURE 1. V—I CHARACTERISTICS BSR SWITCHING

II. REVIEW OF LITERATURE

It should be noted here that only published information is reviewed. Considerable research has been done in BSR that has not been published. Since both inorganic and organic materials exhibit BSR phenomenon, the review will follow the chronology in each area separately.

BSR in crystalline stibnite (Sb_2Se_3) with excess anitmony was reported by Davis and Gildart (2) of University of Kentucky in 1958. They observed bulk resistivity of stibnite decreased abruptly by six order of magnitude as the applied voltage reached a threshold value. The reverse transition was induced by heating the material to 300°C. In 1961 a patent was filed by S. Ovshinsky (1)[1] an independent inventor, on symmetrical current control devices which included BSR devices. Ovshinsky made his devices from materials of group IVA, VA and VIA and many other glass compositions. In 1962 Pearson, Northover, Dewald and Peck (3) of Bell Telephone Laboratories detected BSR in As-Te-I glass. They reported both transitions, i.e. R_h to R_l and R_l to R_h could be induced by electrical signals. Cline (4) of Sandia Corporation observed BSR in anodized aluminum film in 1962. From 1963 to present various authors reported the observations of BSR in NiO (5), Nb_2O_5 (6) and VO_2 (7). Work with organic materials started at Diamond Ordnance Laboratories in the late 1950's in search for a reusable fuse. This work was picked up by Sawyer, McCarthy and Jacoby (8) of Sandia Corporation in 1960. They experimented with an

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[1] Energy Conversion Devices, Inc. was founded by S. Ovshinsky and marketed a family of current control negative resistance device called Ovonic Threshold Switch and a family of bistable memory devices called Ovonic Memory Switches.

electronically activated switch by imbedding aluminum powders in an epoxy binder. In 1961, Mathews (9) of Iowa State University prescribed the curing agent and the curing process that is necessary for aluminum powder filled epoxy bulk to exhibit BSR. In 1967 the author measured BSR in a thin epoxy film without the aluminum powder, as reported in the Sixth Annual Report of Affiliate Program in Solid State Electronics of Iowa State University. Mathew's formula was followed in curing the epoxy film.

III. MATERIAL AND METHOD OF FABRICATION

The initial material evaluated for a memory cell was a thin epoxy film following Mathew's prescription (9). BSR was measured in a one micron thick epoxy film attained by spinning the film substrate at 5000 rpm while curing the film. The film switched satisfactorily with a point contact probe. However, it was found difficult to fabricate an epoxy film of uniform thickness onto a conductor array. Then attention was turned to inorganic materials. The first inorganic material considered was As-Te-I glass as described by Pearson, Northover, Dewald and Peck (3). Decomposition of the material sets in after a few switchings particularly at high current level. It was suspected that some of the iodine sublimated. In 1968 Ovshinsky (10) disclosed that reproducable BSR was observed in As-Te-Ge glass. The glass forming composition range for the As-Te-Ge system was found in works published by Hilton (11) of Texas Instruments who was using it for infrared window. Four different compositions of As-Te-Ge glass were prepared and measured for BSR. These four points as shown in Figure 2a are located on the ternary diagram of As-Te-Ge which was constructed by Hilton. The glass composition that switched more consistently than the others had the following atomic percent of the elements: As 55%, Te 35%, Ge 10%. It has a softening temperature of 240^{o}C. This bulk glass was evaporated into thin film form. All glass film discussed in this thesis will be of this composition.

A. Glass Preparation and Film Evaporation

The As, Te and Ge were weighted and placed in a quartz tube. The tube was evacuated with a mechanical pump for about five minutes and

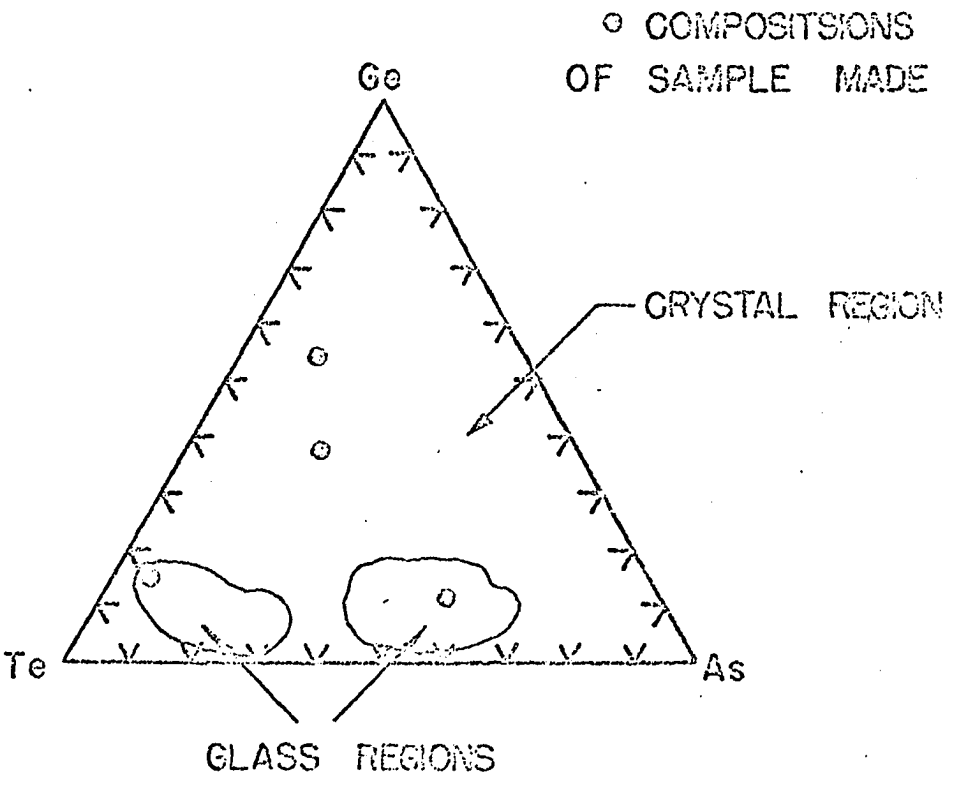


FIGURE 2a. THE As-Te-Ge COMPOSITION DIAGRAM (AFTER A.R. HILTON)

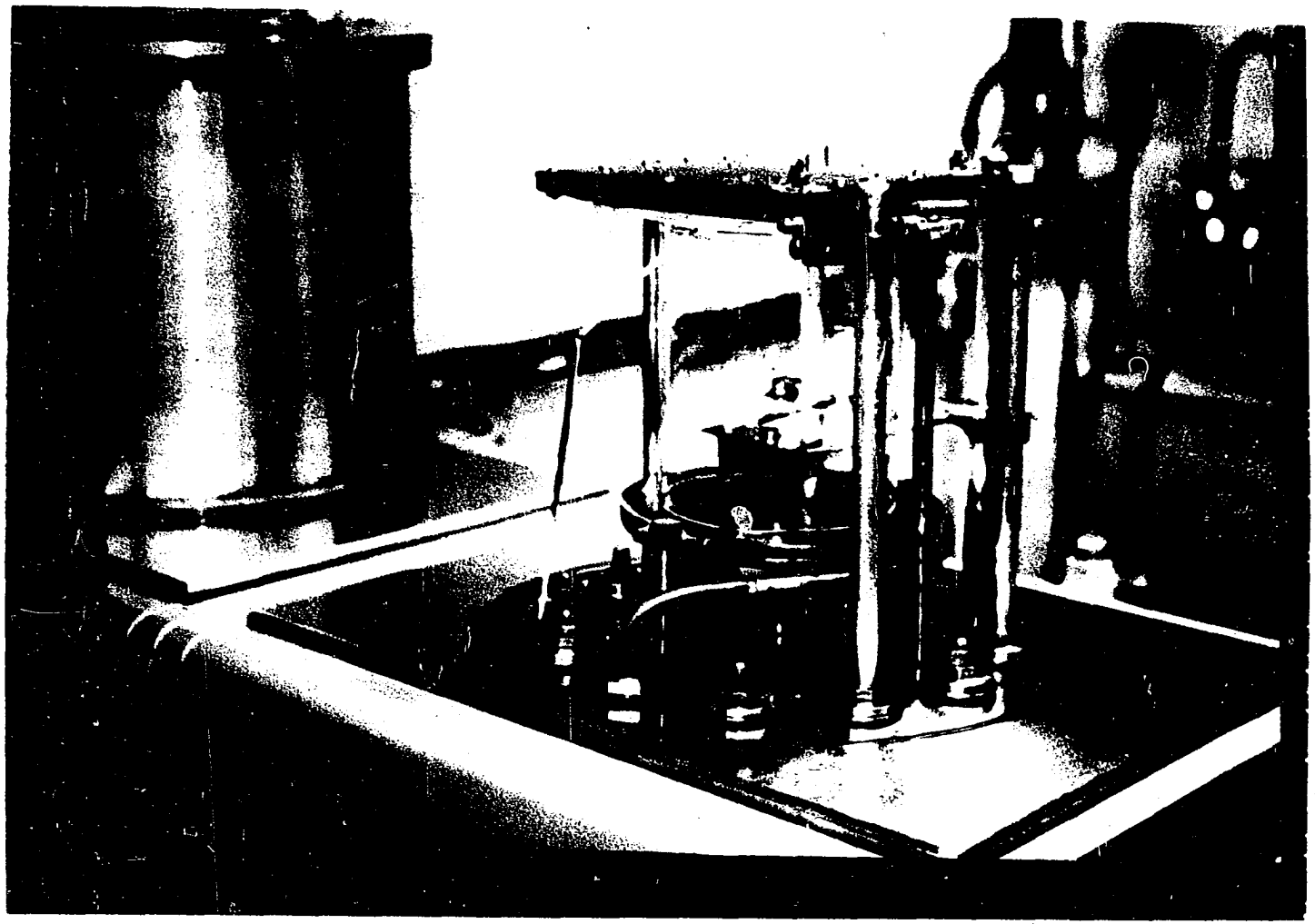


FIGURE 2b. EVAPORATION SET-UP WITH PYREX GLASS CYLINDER

sealed with a hydrogen torch. The tube then was placed in a rocking furnace at 1000°C for about twenty four hours. At the end of this period it was lifted out of the furnace and quenched in air at room temperature. The glass was checked for BSR with a point contact probe and a ground plane. At first the bulk glass material was evaporated from a covered tungsten dimple boat in a vacuum of 10^{-5} Torr onto a substrate which was located five inches above the boat. The temperature of the boat was gradually raised to 1100°C in about twenty minutes. Three undesirable reactions were observed after the evaporation. First is that the glass material alloyed with the boat. Secondly fractionation of the glass was occurring during the evaporation and lastly the film that was on the substrate eventually peeled off after the vacuum was opened. Hence the procedure was modified for subsequent evaporation to remedy these faults.

A molybdenum multibaffle furnace boat was substituted for the covered dimple boat. A thin layer of calcined alumina powder in water suspension was sprayed onto the inner surface of the boat. The boat was outgassed at 1600°C for ten minutes in vacuum. The glass was ground into powder form and sifted through a a 100 mesh screen before it was loaded into the boat. A pyrex cylinder, obtained by cutting off the bottom of a 2000 ml beaker, was used to enclose the evaporation source and the substrate surface as shown in Figure 2b. During evaporation the substrate temperature was held at 100°C and the boat was heated to 1100°C within fifteen seconds and all the material in the boat was evaporated instantaneously. Films evaporated by the modified procedure described above were satisfactory both electrically and mechanically. Subsequent micro-probe analysis of the films indicated no fractionation occurred during evaporation. The evaporated films were also examined by 1) X-ray

diffraction, 2) electron microscopy of surface replica and 3) optical microscopy of chemically etched surfaces. All results confirmed the films to be amorphous.

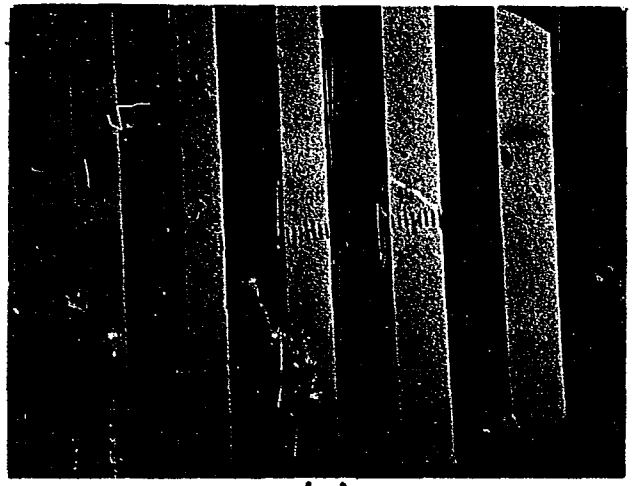
B. Array Fabrication

Besides the main objective to ascertain the switchability of the As-Te-Ge film at the intersections of the orthogonal conductor array, other practical questions were answered by fabricating a test array, such as to determine the adherence of evaporated aluminum conductors on As-Te-Ge film. A 1"x1"x0.038" microscope slide glass was used for the test array substrate. The substrate was cleaned and a 200Å of chromium and 3000Å of aluminum were evaporated through a wired mask with an electron beam gun. This provided an array of 2 mil wide metallizations with a 4 mil center to center distances as shown in Figure 3a. This particular wire mask was used because it was readily available. A 5000Å continuous As-Te-Ge film was evaporated onto the substrate as shown in Figure 3b using the procedure described in III-A. The array fabrication was completed by a last evaporation of 3000Å aluminum conductors through the same wire mask but positioned orthogonal to the first layer conductors. This is shown in Figure 3c. Visual inspection of the array through microscope as evidenced by Figure 3c indicated good adherence of evaporated aluminum to As-Te-Ge film.

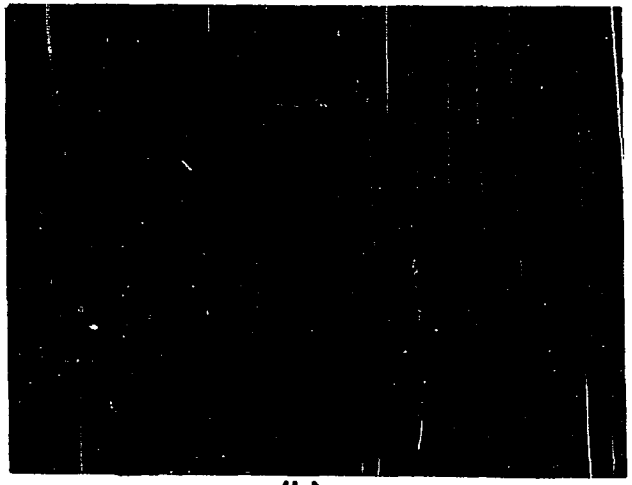
C. Measurements

The BSR was displayed on a Textronic 575 curve tracer. In measuring bulk materials, a chip of the glass was placed on a cleaned flat aluminum

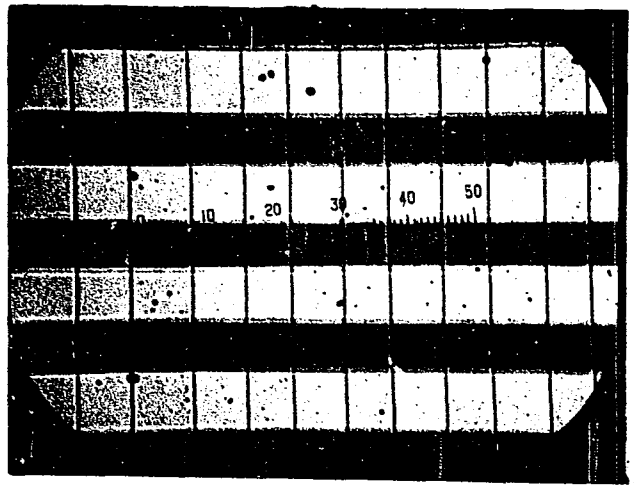
Figure 3 Evaporated array
(a) First layer of Cr-Al metallization (white areas) on glass slide, (b) 5000Å of As-Te-Ge on top of (a), (c) Al metallization (brightest areas) orthogonal to (a) on top of (b), (d) typical V-I characteristics of an intersection



(a)



(b)



0.1mm/ division (c)

(d)

FIGURE 3 (a) FIRST LAYER OF Cr-Al METALLIZATION (WHITE AREAS) ON GLASS SLIDE. (b) 5000Å OF As-Te-Ge ON TOP OF (a). (c) Al METALLIZATION (BRIGHTEST AREAS) ORTHOGONAL TO (a) ON TOP OF (b). (d) TYPICAL V-I CHARACTERISTICS OF AN INTERSECTION.

substrate which was used as a ground plane. The point contact was made by a Micro-Tech Model 2080 Manual Needle Probe. A tungsten carbide needle probe has a radius of 0.5 mil and can be lowered with a vernier control. In measuring BSR in film, the point contact described above and the conductive substrate ground plane were used. Both the glass bulk and the glass film were checked for BSR prior to use the material for array fabrication. Typical measured R_h and R_l values of 5000Å thick As-Te-Ge film were $3x10^6$ ohms and 100 ohms respectively.

In measuring the array device characteristics electrical connections were made to the two orthogonal conductors with the Micro-Tech Model 2080 Needle Probe. The measured V-I characteristics of an intersection is displayed in Figure 3d. Here it should be noted that the measured high resistance value, $R_{h_{measured}}$ is not the true R_h of the intersection, because of the sneak path coupling of the high resistance of all other intersections of the array. For an array with m column and k row, R_h and $R_{h_{measured}}$ can be related as

$$R_h = R_{h_{measured}} \left[\frac{mk}{m+k} + 1\right] \qquad (1)$$

assuming $m+k \gg 1$. This relation will become self evident by inspecting the equivalent circuit of the array as shown in Figure 11. The fabricated array had 250 columns and 92 rows. The slopes in Figure 3d indicated that R_l = 100 ohms and $R_{h_{measured}}$ = 12.4k ohms for a 2 mil x 2 mil intersection. By using Equation 1 true R_h of the intersection can be calculated to be 244k ohms.

In comparing the measured R_h and R_l of the array devices (244k ohms and 100 ohms) with that of the point contact probe ($3x10^6$ ohms and 100

ohms), it is interesting to note that the R_h varied approximately inversely with the cross section area of the device while R_l remained invariant with respect to the cross section area of the device. This implied that the R_h is a measure of the bulk resistivity of the As-Te-Ge glass film in its high resistance state and the low resistance state extended over a filamentary volume of the film. Using the observed radius of the indentation made by the contact probe as the upper limit, the radius of the low resistance filament is no more than 0.1 mil. At some but not all intersections of the array the threshold voltage and current values stabilized to some quiescent values after a few switches. However, once V_t and I_t were stabilized they were very reproducible. The BSR switching is much more consistent in array device than the point contact device. Typical measured V_t and I_t of the array device were 4 V and 8 mA. As will be shown later a non-linear circuit element such as diode, transistor or IGFET are needed for BSR memory array sneak path noise reduction; the physical size of the isolation elements determines the memory density. In planar process of fabricating an integrated diode array, a photolithographic technique is used to selectively etch the SiO_2 layer which is thermally grown on top of the silicon chip in an oxygen atmosphere. Then the SiO_2 layer is used to mask the impurity diffusion. With the planar process of fabricating P-N junction diode arrays, it is within the present state of art to achieve a density of 2.5×10^5 diodes/in^2. Such a diode matrix might have a cross over junction area of 1 mil x 1 mil and a center to center distance of 2 mil. Therefore, a memory density of 2.5×10^5 bits/in^2 is achievable as far as

fabrication technique is concerned. With these array dimensions the following device characteristics will be used in evaluating memory array properties in the next section.

V_t = 4 V $\qquad$ I_t = 8 mA

$R_h = 10^6$ ohms $\qquad$ R_l = 100 ohms

The analysis in the next section shows the necessity of connecting a diode or other device in series with the BSR device for back coupling isolation. Consequently, to achieve isolation a 5000Å As-Te-Ge glass film was evaporated onto the emitter base junctions of a Fairchild 914 IC chip mounted in a TO-5 can. A point contact probe was used to measure the switching action of the emitter base diode junction in series with the As-Te-Ge film. Satisfactory and repeatable BSR switching was observed. The resultant V-I characteristic was essentially that of a diode in series with R_h or R_l, as shown in Figure 4. The V_t and I_t of the device were 18 volts and 10 mA respectively.

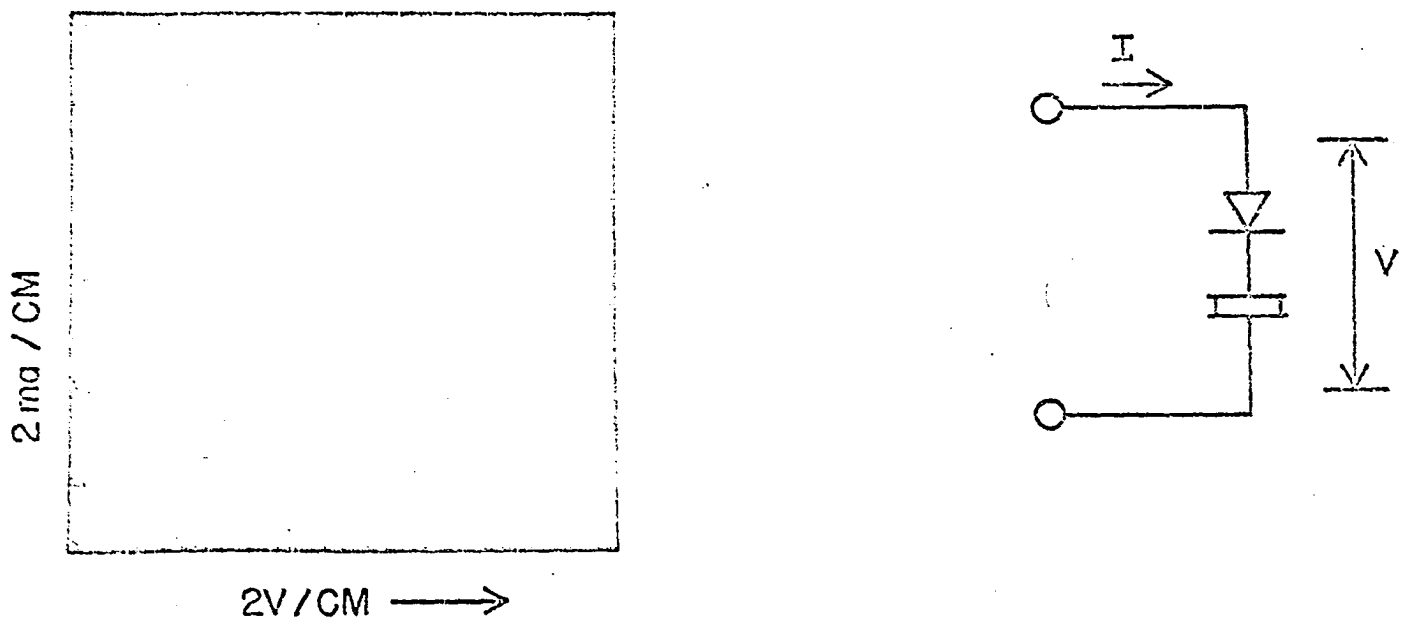


FIGURE 4. V-I CHARACTERISTICS OF A BSR DEVICE IN SERIES WITH A PN JUNCTION DIODE, THE BSR DEVICE IN HIGH RESISTANCE STATE (HORIZONTAL TRACE) IN LOW RESISTANCE STATE (VERTICAL TRACE).

IV. MEMORY ARRAY PROPERTIES

The memory array properties of an electrically changeable read only memory will be considered with the measured device characteristics of the BSR. The basic characteristics of an electrically changeable read only memory are:

1. The read out is non-destructive.
2. The word lines are randomly accessible.
3. The read cycle time should be much faster than the write time.
4. Different read and write drivers can be tolerated.

Read only memories typically are used for 1) control memory in a microprogrammed machine, 2) table look up, and 3) code emulation. A microprogrammed machine contains a main memory and a control memory (12). The control memory replaces much of the wired-in control logic circuitry which decodes the instructions and executes the desired functions. The basic machine characteristics are predominately determined by the nature of the instruction code and with an electrically changeable read only memory in a microprogrammed machine, it is possible to alter the code and the area of optimized performance.

The dominant problem to be considered in building a memory array with linear, two terminal devices, such as the BSR element, is the back coupling or sneak path noises. The undesirable back coupling from the digit sense line to the word line creates two types of problems which can be best illustrated by the memory array schematics as shown in Figure 5. The memory is organized into a 2D array that is m word lines which are orthogonal to k digit sense lines. The selection of a word

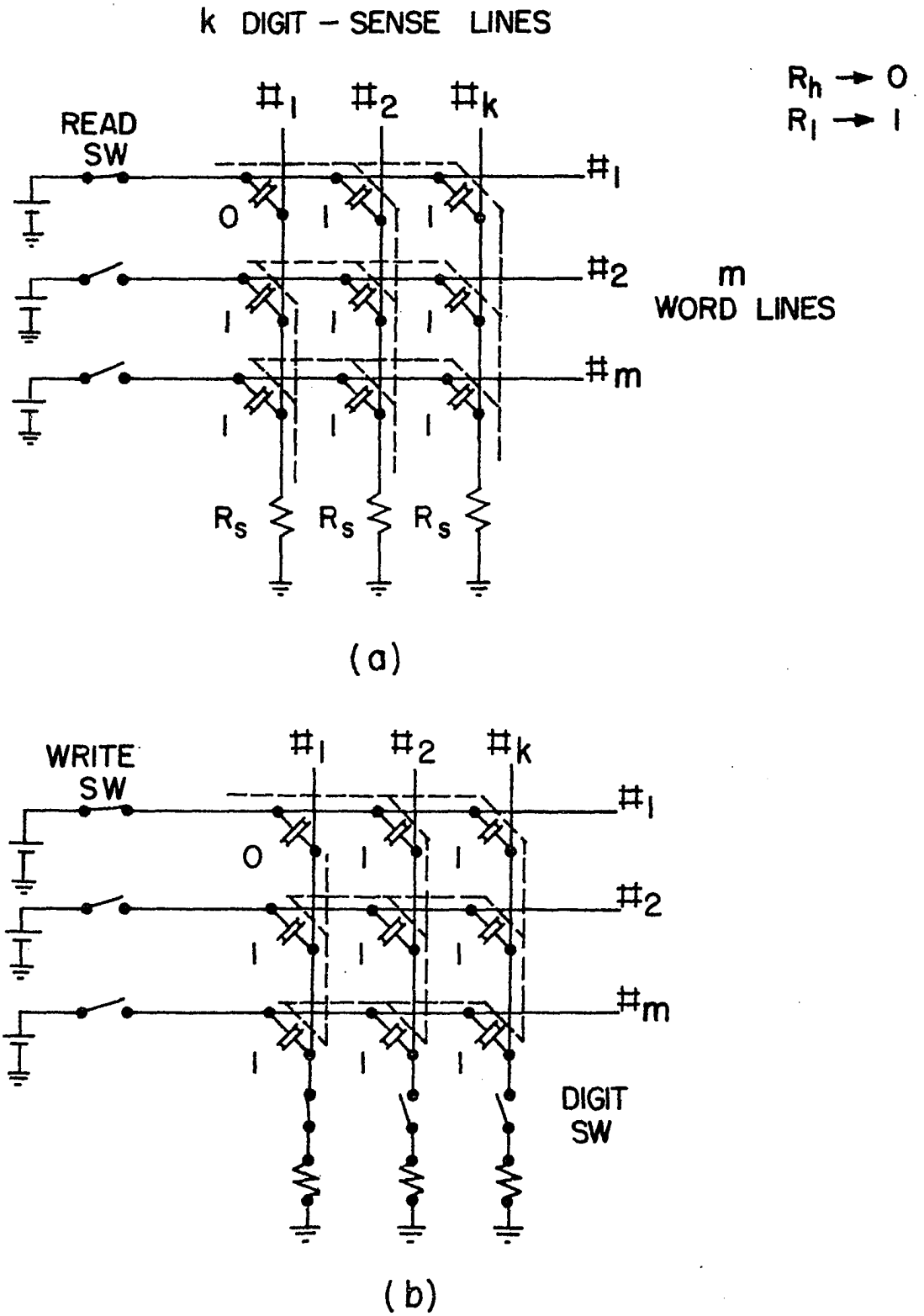


FIGURE 5. SNEAK PATHS DURING (a) READ CYCLE (b) WRITE CYCLE

line causes k bits to be read out in parallel. During the read cycle as shown in Figure 5a, the back coupling from the sense lines to the word lines can cause the 0 located at #1 digit sense line to be read out as 1. During the write cycle as shown in Figure 5b all the intersections in the 1 states or in the low resistance states would present a loading problem to the writing of 1 into the bit located at intersection of #1 digit sense line and #1 word line. To circumvent these problems, it is necessary to introduce a nonlinear circuit element such as diode in series with the BSR storage cell in order to isolate the back coupling from the sense line to the word line. These problems can be examined more closely only after the BSR device is characterized. Then, an equivalent circuit of the array will be constructed and some projections will be made on memory array size in terms of device parameters and driving schemes.

A. Device Characterization

Before memory array properties can be ascertained, the BSR device itself must be characterized. The BSR device with its external circuit elements, V_s and R_c are shown in Figure 6. With R_c as drawn on the V-I curve, two loop equations of the circuit can be written for the high and low resistance states as follow

$$V_s = I_1 R_c + I_1 R_h \tag{2}$$

$$V_s = I_t R_1 + I_t R_c \tag{3}$$

and R_c can be solved from Equation 2 and Equation 3 as

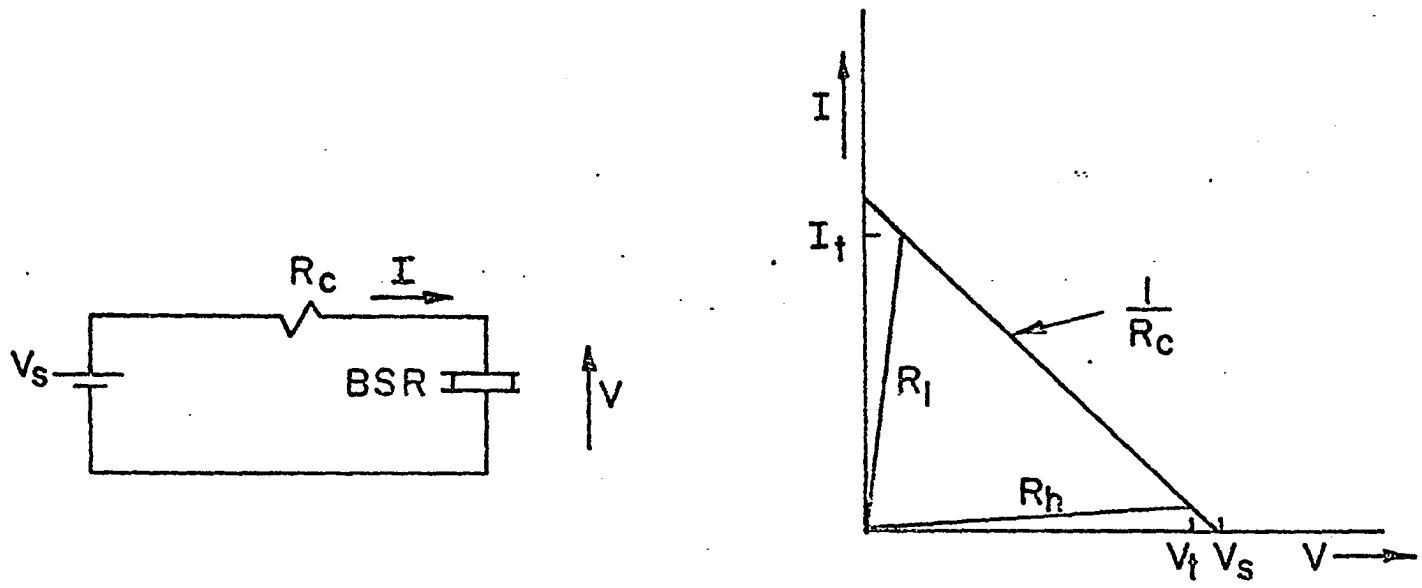


FIGURE 6. CRITICAL RESISTANCE LOADING

$$R_c = \frac{V_t - I_t R_l}{I_t - \frac{V_t}{R_h}} \tag{4}$$

R_c is defined as the critical resistance of the device. That is to say for switching from R_h to R_l the external load resistance must be equal to or greater than the critical resistance and for the inverse transition must be smaller. A small value of R_c signifies the device's tolerance to loading effect.

It would be interesting to examine the effect of an added series isolation resistance, R_I, to the critical resistance value. R_{cI} will denote the critical resistance value of the device with an added series resistance, R_c, as shown in Figure 7. Similar to Equation 1 and Equation 2

$$V_s = \frac{V_t}{R_h}(R_{cI} + R_I + R_a) \tag{5}$$

$$V_s = I_t(R_l + R_{cI} + R_I) \tag{6}$$

and

$$R_{cI} = \frac{\frac{V_t}{R_h}(R_h + R_I) - I_t(R_l + R_I)}{I_t - \frac{V_t}{R_h}} \tag{7}$$

By using Equation 4

$$R_{cI} = R_c - R_I \tag{8}$$

which showed that the critical resistance of a device can be reduced by the addition of series resistance as indicated by Equation 8.

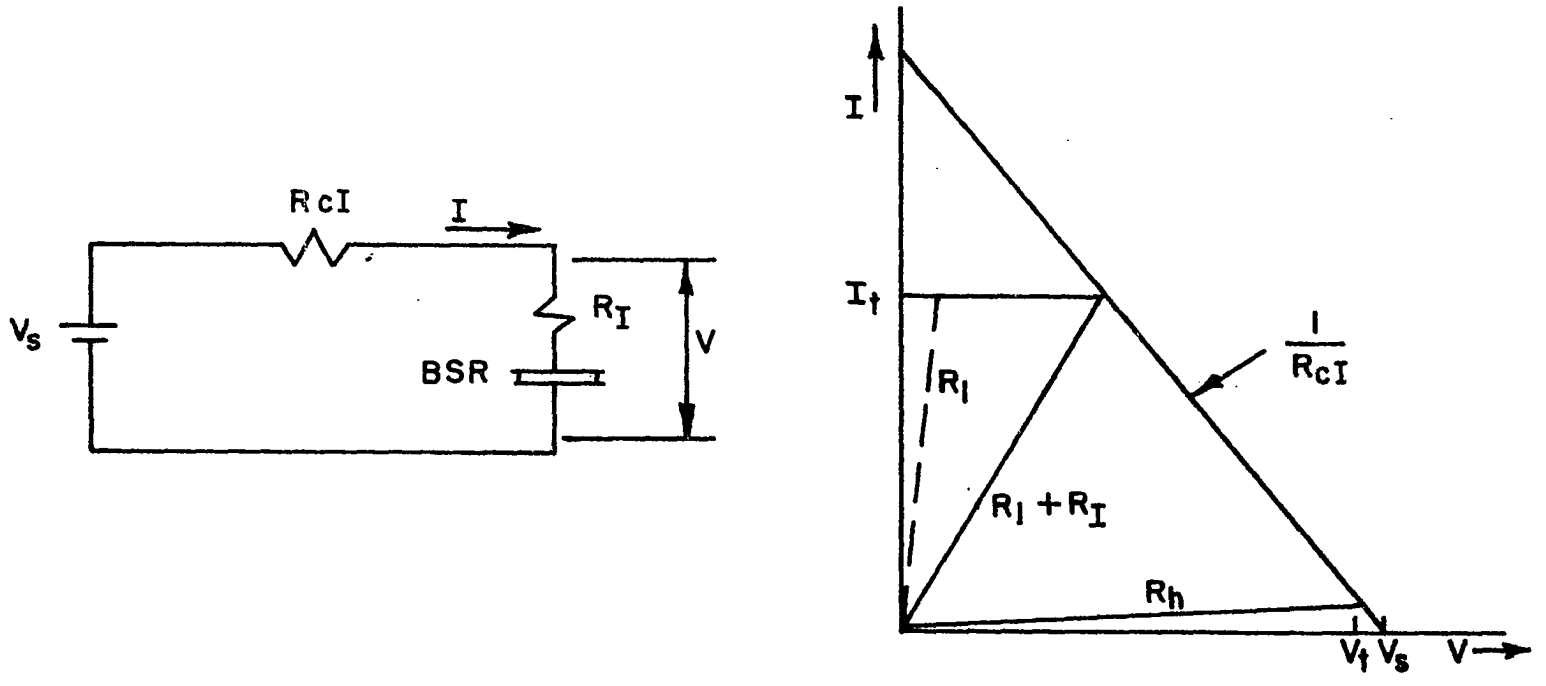


FIGURE 7. CRITICAL RESISTENCE LOADING WITH SERIES ISOLATION RESISTENCE

B. Loading Considerations

The effect of backcoupling loading on the switching of BSR device is characterized by the equivalent circuit as shown in Figure 8. V_s and R_s are the applied voltage and source resistance for writing. R_T is the total resistance of all other intersections of the array connecting through the backcouplings. It is assumed here that all word lines and digit sense lines of the array are opened except the activated word line and digit sense line. Therefore, R_T will determine the maximum allowable array size. The worst case conditions for switching a BSR device from R_h to R_l are

$$\frac{V_s R_T}{R_T + R_s} \geq V_t \tag{9}$$

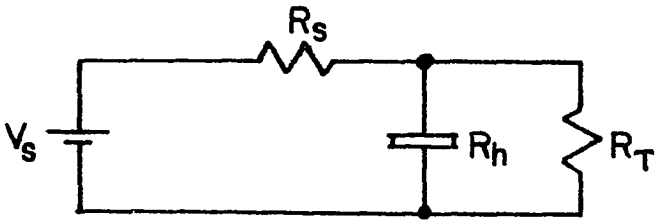
and

$$\frac{V_s}{R_s + R_l} \leq I_t \tag{10}$$

Since the measured R_h is $10^6\Omega$ the approximation $R_T \ll R_h$ is made in Equation 9. Equation 9 indicates that the applied voltage across the device with a parallel load of R_T, must be greater than V_t for switching from R_h to R_l. Equation 10 states that once the device is switched to R_l, the maximum current in the device must be lower than I_t with R_T removed. Combining Equation 9 and Equation 10 the following inequality is obtained.

$$\frac{R_s R_T}{R_s + R_T} \geq R_c + R_l\left(1 - \frac{R_T}{R_T + R_s}\right) \tag{11}$$

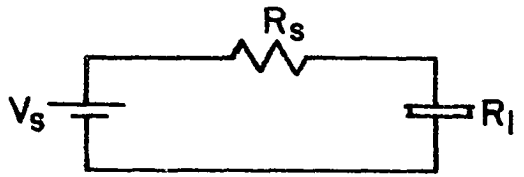
where R_c is the critical resistance of the device as defined by Equation 4.



DEVICE PARAMETERS R_b, R_l, V_t, I_t

CIRCUIT PARAMETERS V_s, R_s, R_T

(I) $\quad \frac{V_S R_T}{R_t + R_s} \geq V_t$



(II) $\quad \frac{V_S}{R_s + R_l} \leq I_t$

FIGURE 8. EFFECT OF LOADING (R_T) ON SWITCHING FROM R_h TO R_l

It is interesting to note that Equation 11 indicates that limits imposed by Equation 10 is actually a more stringent condition than Equation 4 Thus, limits imposed by Equation 9 and Equation 10 are the worst case write requirements.

By substituting the measured device parameters (V_t = 4V, I_t = 8mA, R_1 = 100 ohms, $R_n = 10^6$ ohms) into Equation 9 and Equation 10, R_s and R_T are plotted against V_s in Figure 9. The dotted lines are for device parameters with $\pm$ 10% tolerances.

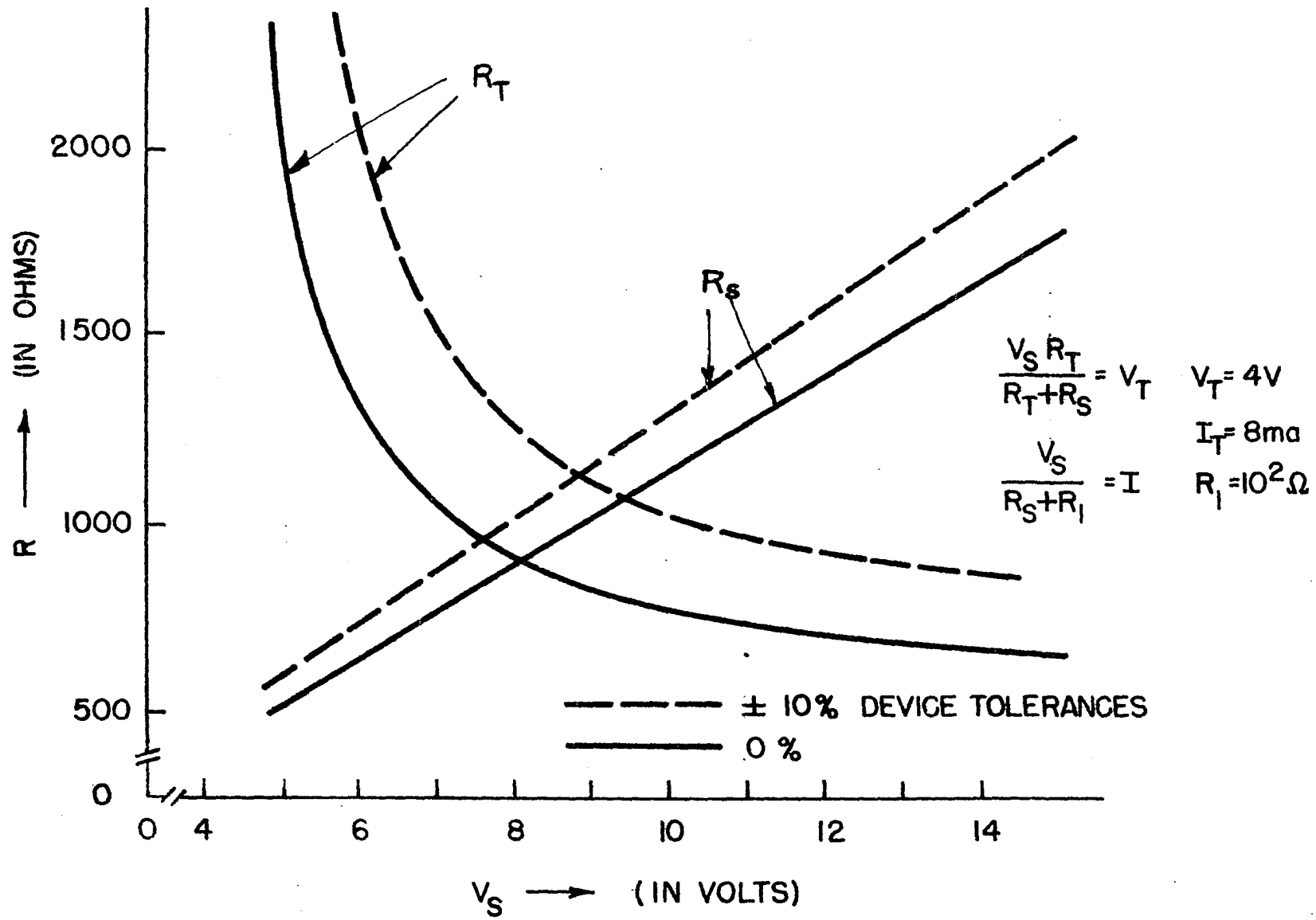
Let's assume a V_s of 10.3V and a $\pm$ 10% tolerance on device parameters. The plot in Figure 9 shows that the R_s should be 1350 ohms and the R_T value should not be lower than 1000 ohms. In otherwords the total resistance loading through backcoupling of the memory array should be higher than 1000 ohms. The maximum loading occurs when all other intersections are in the low resistance state, R_1. This low value of R_T clearly demonstrates the need of isolation. Figure 9 also shows quantitatively that tolerances of device parameters can be overcome by increasing V_s and R_s.

The plot in Figure 9 can be used in making trade-off between memory array size, i.e. R_T, driving power, i.e. V_s and R_s, and device parameter tolerances. It is necessary to relate R_T to the array size. This will be done in the following section.

C. Array with Diode Isolation

The intersection of the array under consideration consists of a BSR device connected in series with a diode as shown in Figure 10. The array is organized in 2D. The write process is bit by bit which means

Figure 9. R_T and R_s vs V_s for $\pm$10% device tolerances


R (IN OHMS)
2000
1500
1000
500
0
0
4
6
8
10
12
14
V_S (IN VOLTS)
R_T
R_S
$\frac{V_S R_T}{R_T+R_S} = V_T$
$V_T = 4V$
$I_T = 8ma$
$\frac{V_S}{R_S+R_1} = I$
$R_1 = 10^2\Omega$
± 10% DEVICE TOLERANCES
0 %

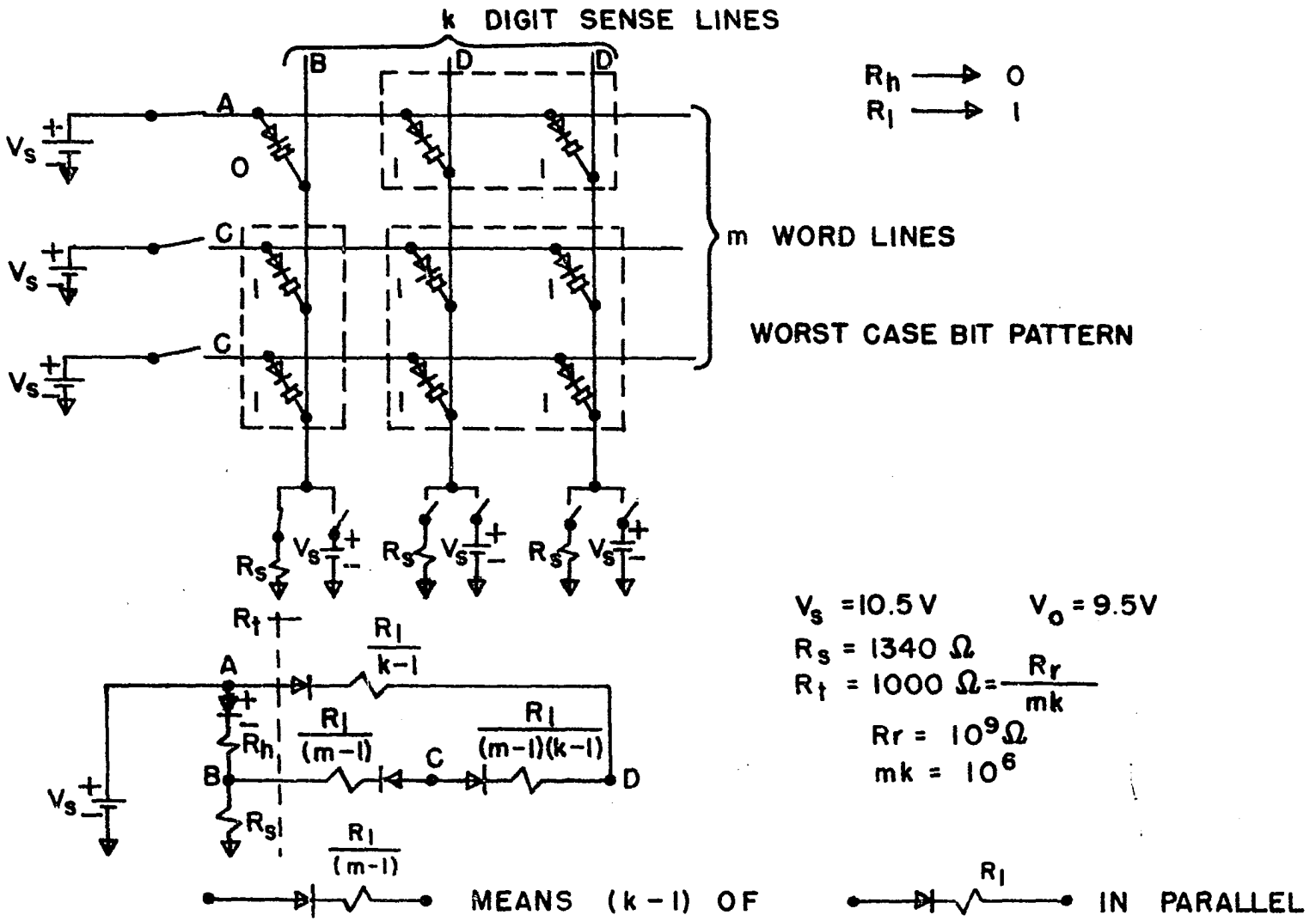


FIGURE 10. WRITE CYCLE WORST CASE CONSIDERATION

that the digit sense line switches are turned on-off sequentially while the word line switch is remained on during the writing of the word. All other word line switches are remained off.

1. Write cycle considerations

Let one define R_h as 0 and R_1 as 1. The worst case bit pattern for write a 1 into intersection AB (from now on AB will stand for intersection AB) is that all other intersections of the array are loaded with 1. Since all word lines except A are at equipotential and all digit sense lines except B are at equipotential it is possible to lump these points to be C and D respectively. Then, the equivalent circuit of the array can be simplified as shown in Figure 10 which clearly indicated that the diodes in DC provides the necessary isolation. The parallel load R_T of Equation 9 is the serial resistance of AD, DC and CB. Since only the diodes in DC are back biased, therefore

$$R_T \cong \frac{R_r}{(m-1)(k-1)} \tag{12}$$

where R_r is the back biased resistance of the diode. Assume $R_r = 10^9$ ohms, which is a realizable figure for silicon junction diode, and use a figure of 1000 ohms for R_T as attained in Section III-B, the array size, mk can be determined from Equation 12 to be 10^6 or $m=k=10^3$.

2. Read cycle considerations

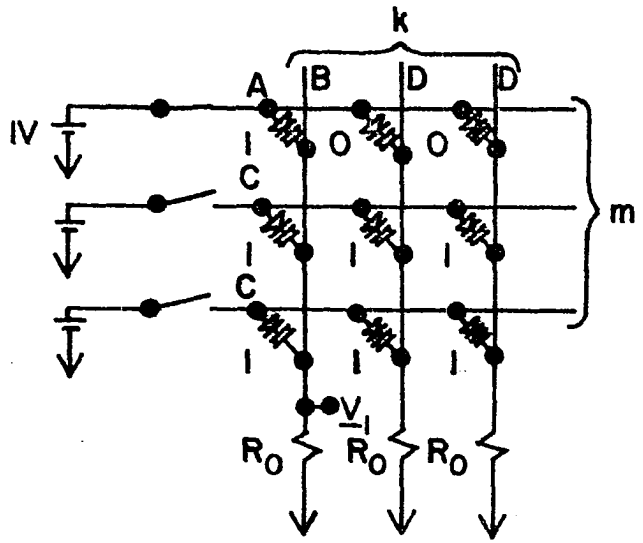
The above section showed that as far as the worst case write cycle is concerned it is feasible to build $10^3 \times 10^3$ array with diode isolation. Now let's consider the same array for worst case read cycle operation. The 10^3 bits of a word line are read out in parallel. During the read

cycle, the two important factors to be considered are the signal to noise ratio, S/N and the amplitude of the 1 signal, V_1. The signal to noise ratio is defined as the ratio of minimum 1 signal to maximum 0 signal. The bit patterns used for S/N calculations are shown in Figure 11. S/N and V_1 are calculated and plotted in Figure 12 as function of the sense line resistance, R_o. The read voltage is assumed to be 1 volt. Since R_o attenuates the sneak path noise more than the 1 signal, S/N decreases and V_1 increases as R_o increases. Chosen R_o to be 50 ohms from the plot of Figure 12 will yield a S/N of 17 and V_1 of 0.3 volt. With these sense signal characteristics, it is possible to drive the memory output logic circuitry with a small amount of amplification. Since the physical dimensions of the array, i.e. 2"x2", are much shorter than distance traveled by the read pulse during its rise time, lumped parameters are used in approximating the transient behavior of the array. The ac equivalent circuit of the memory array (Figure 11) during the read cycle is shown in Figure 13a, where C_B and C_D are the capacitance of the BSR device and the isolation diode respectively. The measured C_B of an isolated 2mil x 2mil junction as shown in Figure 3c is 1.4 pf therefore C_B of a 1mil x 1mil cross over can reasonably be assumed to be 0.35 pf. Typical capacitance of a fast switching diode with low surge current rating is about 0.7 pf. With the following inequalities,

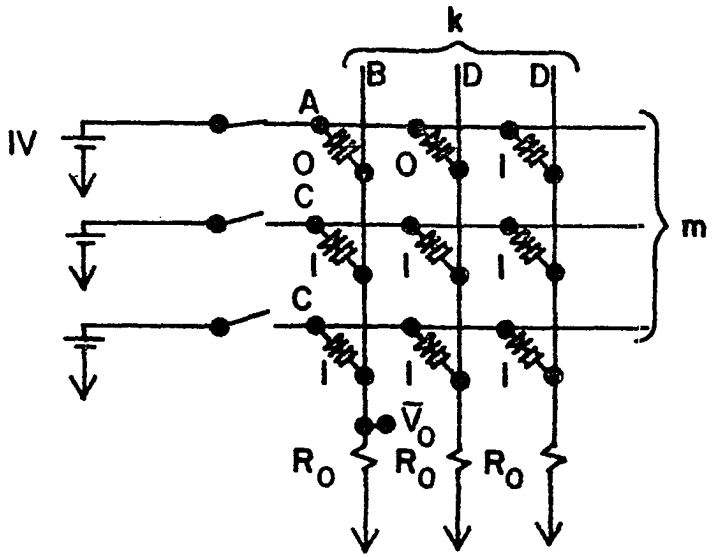
$$R_r \gg R_h,\ R_s \ll R_r/m,\ C_B \simeq C_D \ll mC_D$$

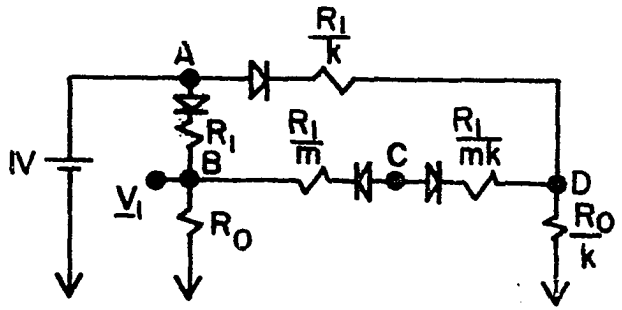
the equivalent circuit of Figure 13a can be simplified to as shown in Figure 13b. For R_s = 50 ohms the time constant of the equivalent circuit is .

BIT PATTERN FOR MINIMUM I SIGNAL, $\underline{V_I}$



BIT PATTERN FOR MAXIMUM O SIGNAL, $\overline{V_O}$





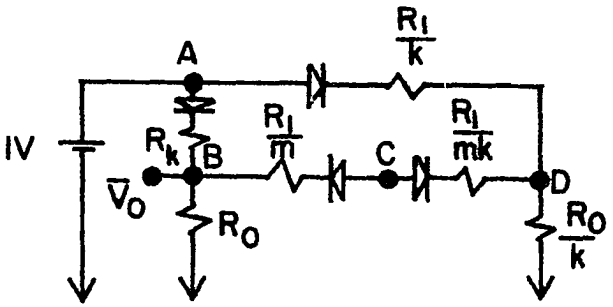


FIGURE 11. READ CYCLE CONSIDERATION

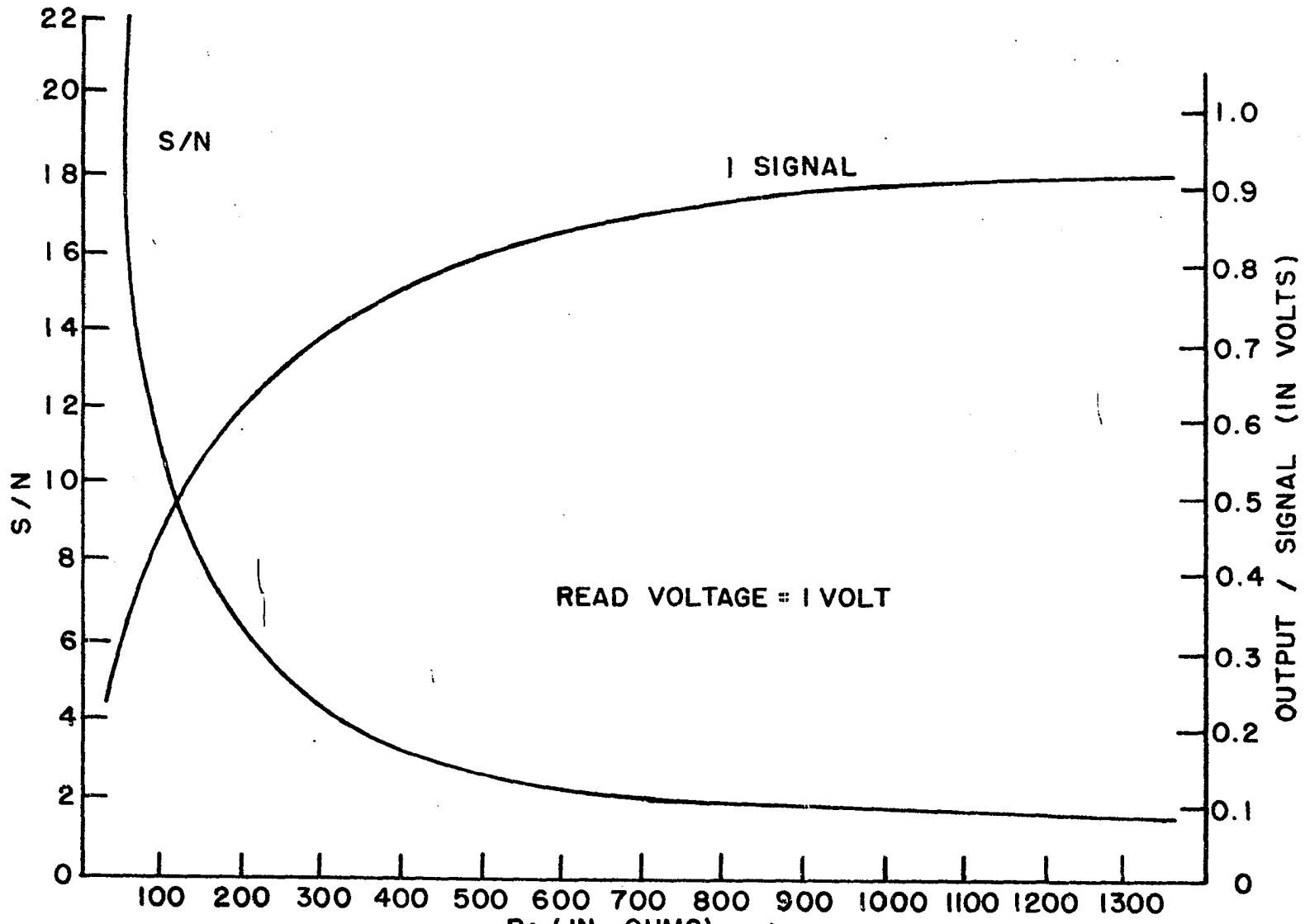
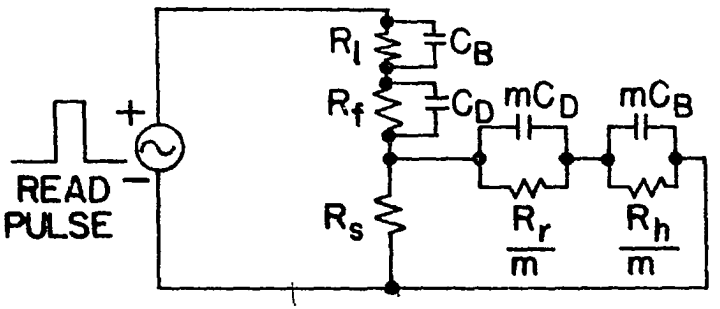
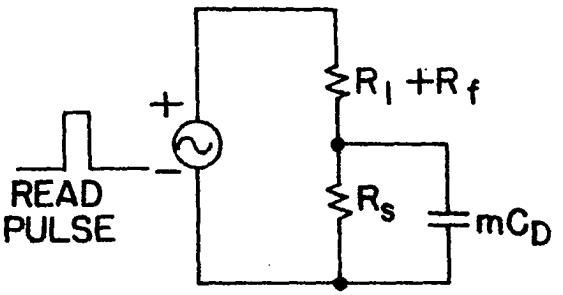


FIGURE 12. S/N AND I SIGNAL vs Ro





$R_l = 100$ ohms $\quad R_s = 50$ ohms

$R_f = 30$ ohms $\quad C_D = 0.7$ pf

$m = 10^3$ $\quad C_B = 0.35$ pf

$$\left[\frac{(R_l + R_f)R_s}{R_l + R_f + R_s}\right] mC_D = 25.2 \times 10^{-9} \text{ sec}$$

(a) (b)

FIGURE 13. (a) A-C EQUIVALENT CIRCUIT OF MEMORY ARRAY DURING READ CYCLE

FIGURE 13. (b) APPROXIMATED CIRCUIT OF (a)

$$RC = [\frac{(50)(130)}{180}][(10^3)(0.7\times10^{-12})]\text{sec}$$

$$RC = 25.2 \times 10^{-9} \text{ sec}$$

Assuming 3RC for the width of the read pulse and 5RC for the discharge of the capacitance, a read cycle time of 200 ns is feasible.

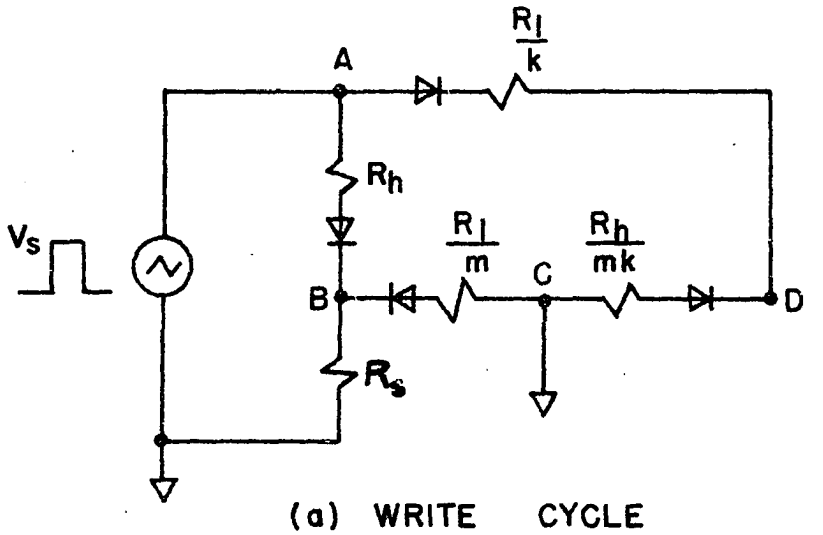
3. Summary of projected array performance

The following are the read-write characteristics of an array with diode isolation. It should be noted here that array with other read-write characteristics can also be interpreted from the plots of Figure 9 and Figure 12.

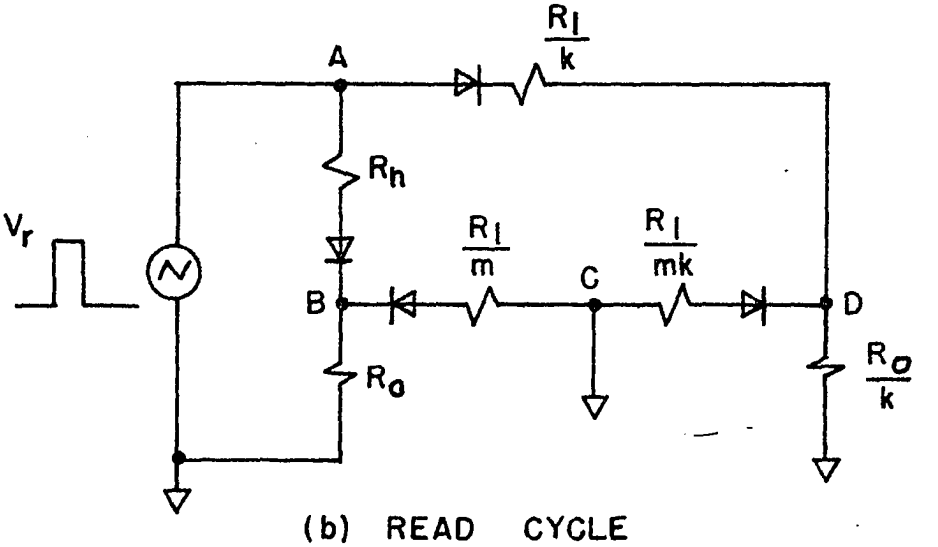
Array Size	10^3 words x 10^3 bits
Physical Size	(array) 2"x2"
	(bit) 1mil x 1mil
Write Cycle	
Voltage	10.35 volts
Digit Line R	1350 ohms
Read Cycle	
Sense Line R	50 ohms
S/N	16
Cycle Time	200 ns

4. Other schemes to eliminate the sneak path noise

Besides the scheme proposed above, there are two other schemes that can be used to eliminate the sneak path noise. The first one as shown in Figure 14 is to use low impedance word line drivers which effectively ground points C. In contrast to that shown in Figure 8, the effective



(a) WRITE CYCLE



(b) READ CYCLE

FIGURE 14. EQUIVALENT CIRCUIT OF ARRAY WITH LOW IMPEDANCE WORD DRIVER

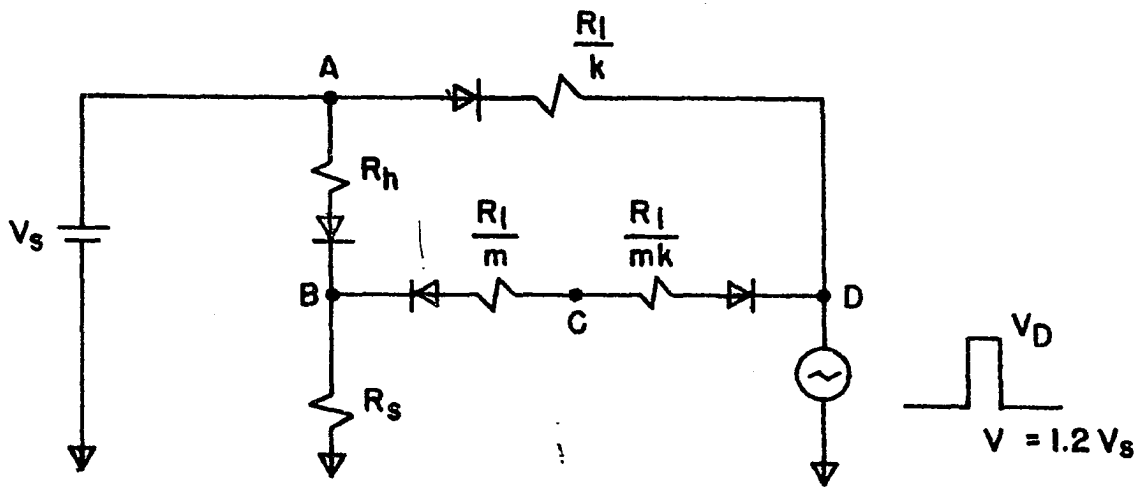
load resistance for the BSR device in AB is R_s in parallel with the back biased diodes in BC instead of R_s in parallel with the back biased diodes in CD. This will extend the memory size by a factor of k. During the read cycle, the S/N and the 1 signal, V_1, will be independent of the bit patterns stored in the array. The S/N and V_1 can be written as

$$\frac{S}{N} = \frac{R_h}{R_o + R_1 + R_f} \tag{13}$$

assuming $R_h \gg R_o$

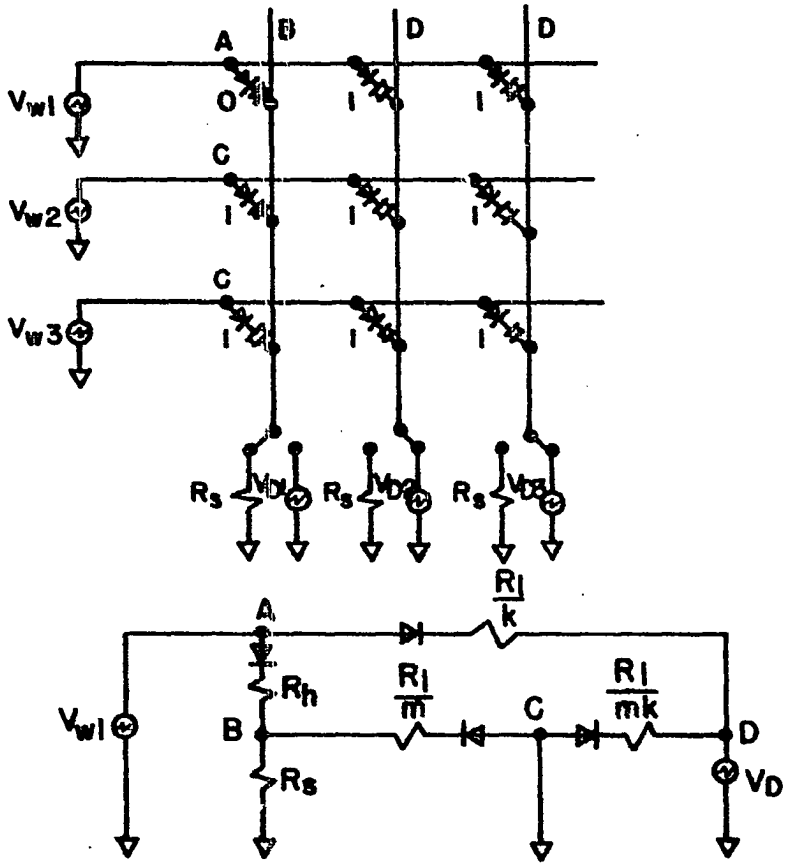
$$V_1 = V_r \frac{R_o}{R_o + R_1 + R_f} \tag{14}$$

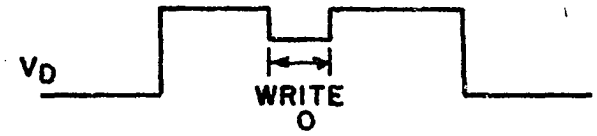
R_f is the forward resistance of the diode and V_r is the word line read voltage. V_r should be constrained such that the voltage and the current in the BSR device be lower than V_t and I_t respectively. The second scheme is to eliminate the sneak path current during writing by back biasing the diodes where the sneak path with digit line voltage drivers noise current flow. In Figure 15, this scheme is used with the on-off word line switches. Here the memory size can be extended because as long as the digit line voltage drivers can supply the diode leakage currents AD and CD will essentially look like current sources and no loading effect will be felt by the BSR device in AB. If this scheme were used with low impedance word line drivers, it would merely reduce the current drain on the word line driver. As shown in Figure 16, the loading on the BSR device in AB would be identical to that shown in Figure 14.



WRITE CYCLE

FIGURE 15. EQUIVALENT CIRCUIT OF ARRAY WITH ON-OFF WORD DRIVER AND BACK BIASING DIGIT DRIVER





READ CYCLE

$$\frac{S}{N} = \frac{R_h + R_s}{R_l + R_s}$$

FIGURE 16. ARRAY WITH LOW IMPEDANCE WORD DRIVERS AND BACK BIASING DIGIT DRIVERS

D. Array with Bipolar Transistor or IGFET for Isolation

Active devices such as a bipolar transistor or IGFET, besides diodes can provide the needed isolation for the BSR storage cell; also they simultaneously serve as amplifying devices during the read and write cycles. This can enable the array to be directly connected between logic stages. The possible arrangements of incorporating active devices with BSR are listed in the following.

The linear select mode with IGFET is shown in Figure 17. The BSR storage cell is connected to the source terminal of the FET. During the write cycle, the word line voltage activates all the FET devices along the word line. The writing of 1 or 0 depends whether the digit line is connected to a current source or a voltage source. During the read cycle the word line voltage again activates the FET, 1 and 0 is sensed respectively by the high and low current levels that flow through the digit line.

The coincident select mode with IGFET is shown in Figure 18. The coincident selection of a X line and a Y line will activate the BSR storage cell which is located at the intersection. The writing of a 1 or an 0 depends on whether a high resistance or a low resistance is connected to the digit line. During the read cycle, the voltage and current that appear across the BSR storage cell should be smaller than the threshold values of the device for non-destructive read out of the memory content.

The linear select mode with the storage cell in the base of a bipolar transistor is shown in Figure 19. In this scheme, separate digit and

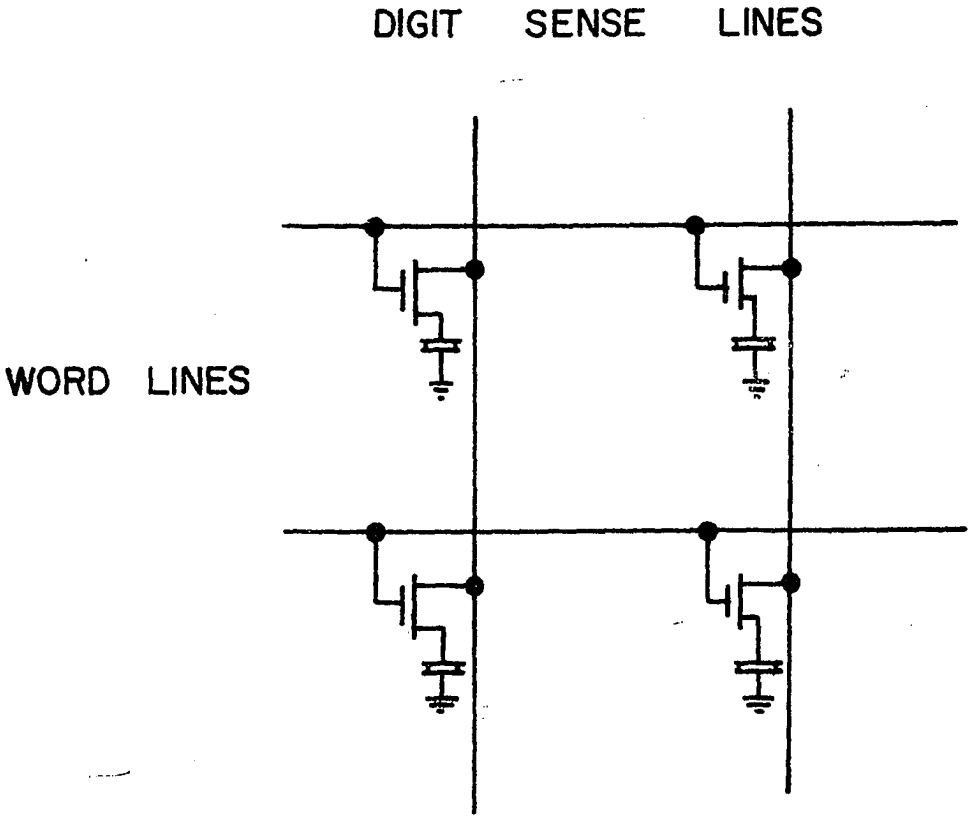


FIGURE 17 LINEAR SELECT IGFET

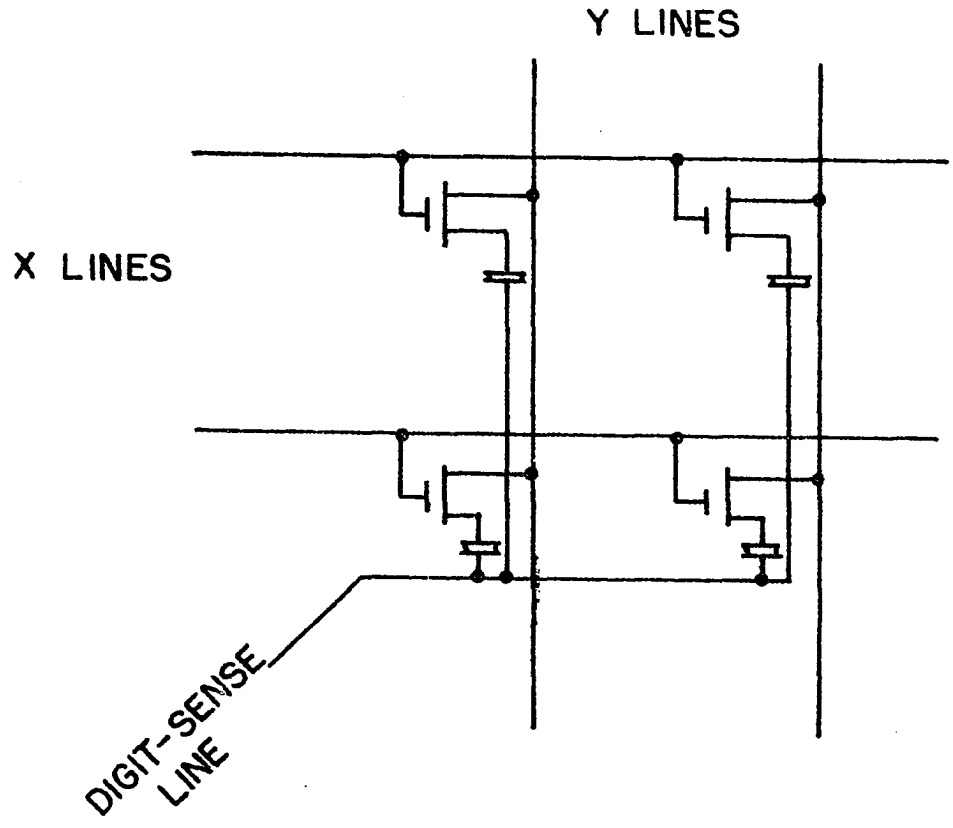


FIGURE 18. COINCIDENT SELECT WITH IGFET

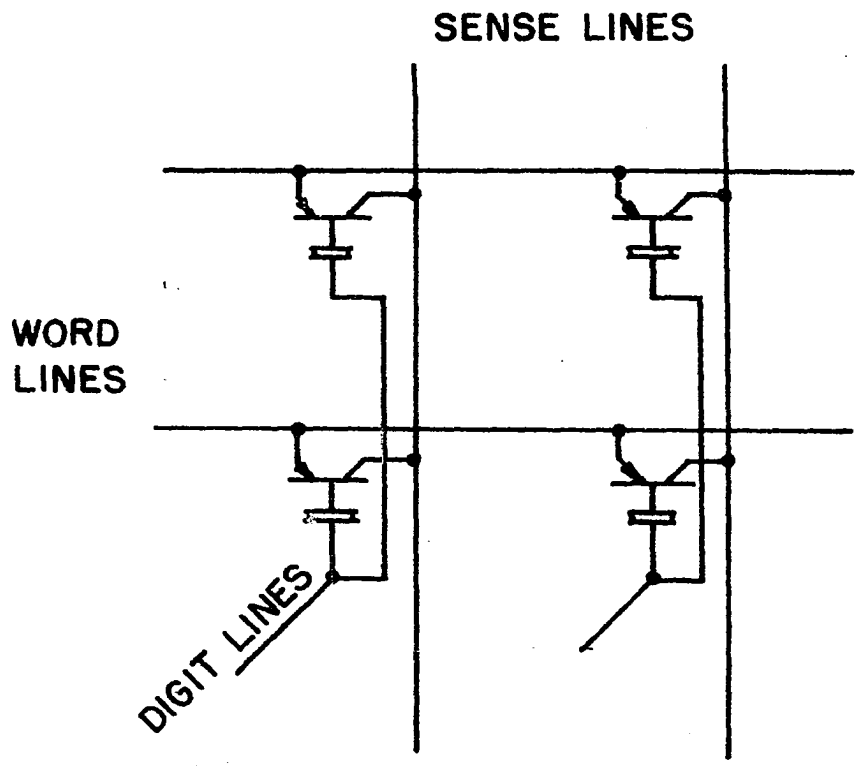


FIGURE 19. LINEAR SELECT WITH CELL IN THE BASE OF BIPOLAR TRANSISTOR

sense lines are needed. During the write cycle, the word line voltage and the appropriate resistance and voltage connected to the digit line determine the writing of 1 or 0 at the intersection. During the read cycle all the digit lines are terminated by a common d-c voltage or ground.

The linear select mode with the storage device in the emitter of a bipolar transistor is shown in Figure 20. This scheme is similar to the first scheme above except that a bipolar transistor is used instead of a FET. Bipolar transistor provides a more efficient switch than FET; that means the resistance between emitter and collector (when the transistor is saturated) is lower than the on resistance between source and drain of a FET.

Coincident select mode with bipolar transistor is shown in Figure 21. Comments made for the scheme just above also apply here.

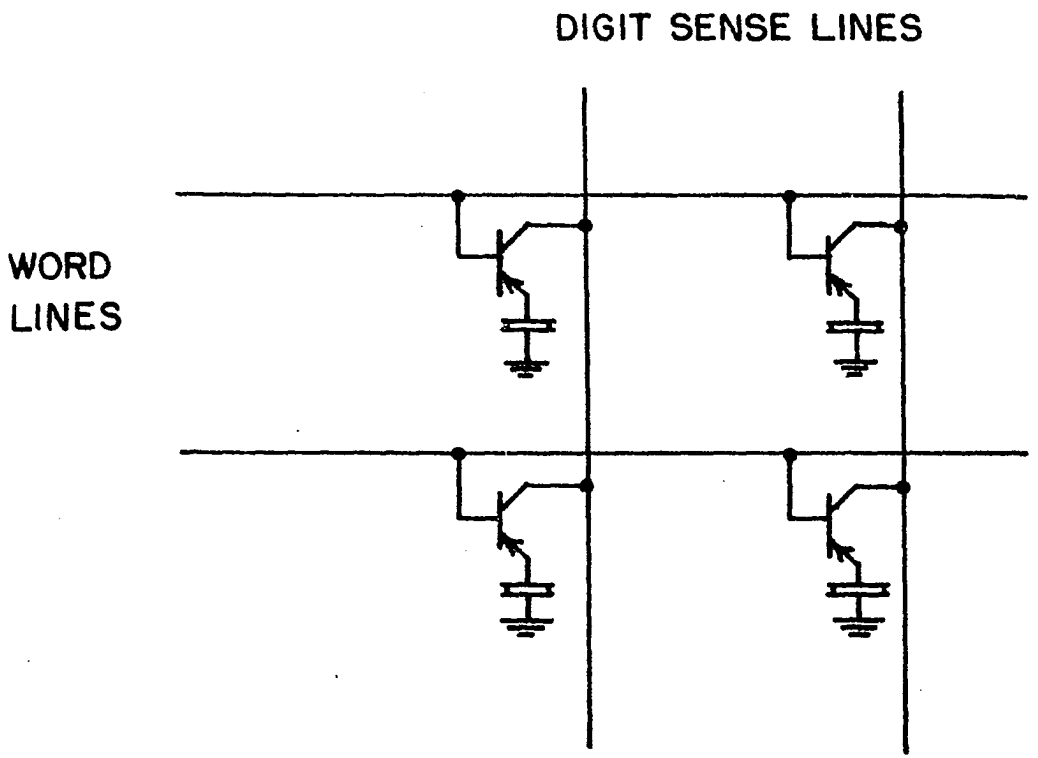


FIGURE 20. LINEAR SELECT WITH CELL IN THE EMITTER OF BIPOLAR TRANSISTOR

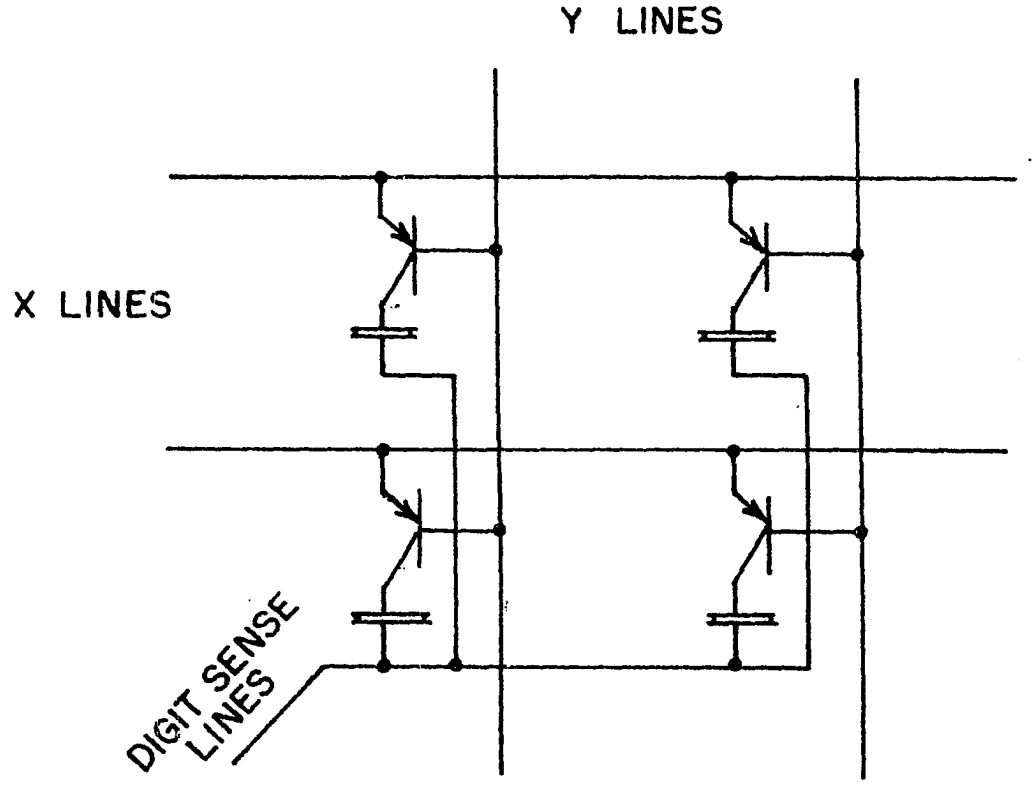


FIGURE 21. COINCIDENT SELECT WITH BIPOLAR TRANSISTOR

V. DISCUSSION

BSR phenomenon exists in both organic and inorganic materials. Due to the complexity of the molecular structure of the organic epoxy film, the phenomenon will be discussed in term of the inorganic As-Te-Ge film. Then an analogy will be drawn between the two materials. It is believed that the BSR switching is a reversible phase transition between the amorphous phase and the crystalline phase.

Before we discuss any results of this thesis research, let's have a brief exposition on published works that are relevant to the explanation of BSR phenomenon. Yin and Regel (13) have measured the resistivity of the random ring structure (amorphous phase) and of the hexagonal chain structure (crystalline phase) of tellurium film; the resistivity differed by about three orders of magnitude. It is interesting to note here that Cuthrell (14) had found m-phenylenediamine cured epichlorhydrin-bisphenol A (exactly identical to the BSR epoxy used in earlier part of this thesis research) can also exist in two different phases depending on the heat transfer rate during curing. This behavior is indeed very similar to that of the inorganic glass. Hatano and Kambara (15) have observed a resistance increase of three orders of magnitude in transition from the crystalline phase to the amorphous phase of the organic polymer, polyacetylene. Accepting the above hypothesis that the resistance switching is a reversible phase transition, then the sequence of events can be illustrated by Figure 22. This hypothesis is further substantiated by the resistance measurements of bulk As-Te-Ge in its amorphous phase and in its crystalline phase. The measured values were

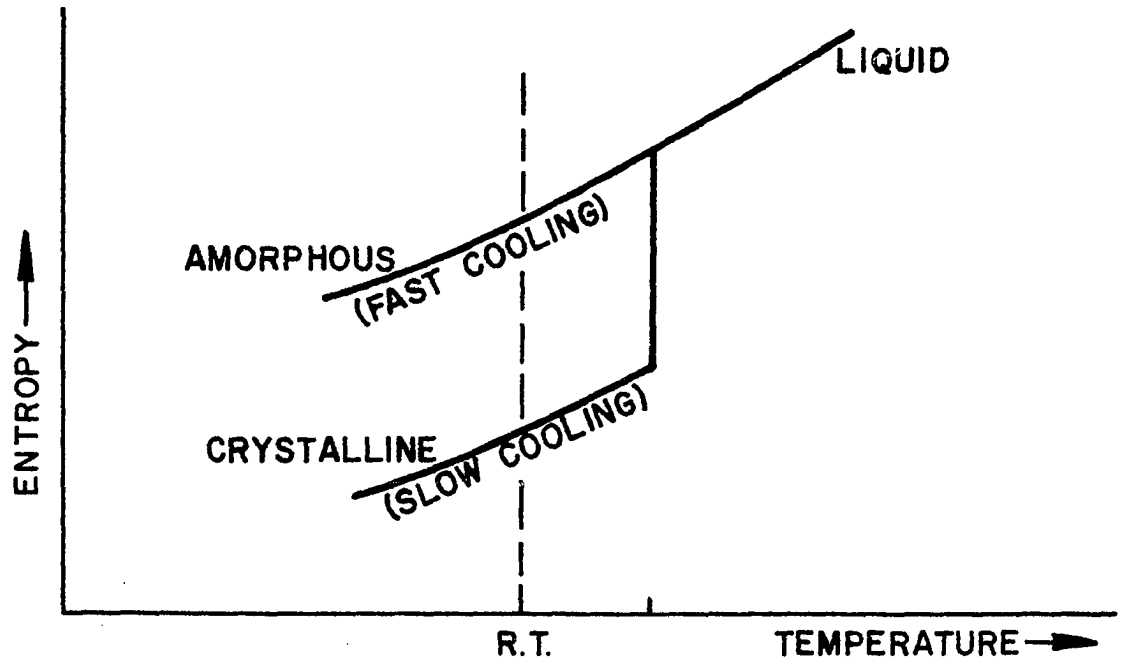
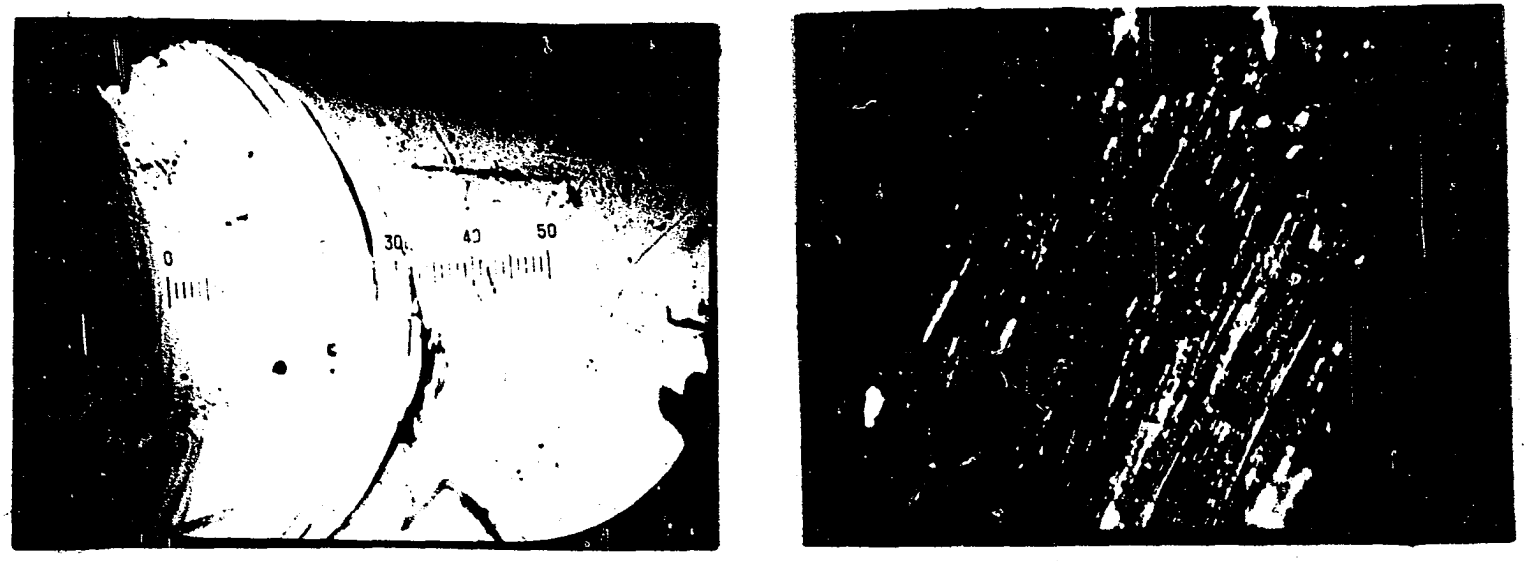


FIGURE 22. TRANSITION DIAGRAM

identical to the R_h and R_l of the BSR device. The material in glass phase was obtained as described in III-A and the crystalline state was induced by heating the glass material to 300°C and let the molten glass cool to room temperature in about 4 hours. Figure 23 shows that the As-Te-Ge in its glass state had a shining and smooth surface while the crystalline state As-Te-Ge had long narrow spiky crystallites (very similar in appearance to the tellurium crystallites) imbedded in a liquid like solid. X-ray diffraction pattern of the above materials in powder form as shown in Figure 24 also confirmed that the materials to be either amorphous or crystalline depending on the quenching condition. However, in the X-ray pattern of the crystalline material amidst the characteristic sharp peaks, there is a broad peak which is typical of glass diffraction pattern. Therefore it is concluded that the crystalline phase is not a pure one; but intermixed with an amorphouse phase. The 2.99Å, 2.15Å and 2.03Å peaks of the diffraction pattern in Figure 24 can be attributed respectively to the 100, 110 and 110 planes of $Ge_{50.8}$ $Te_{49.2}$.

The magnetic susceptibilities of the amorphouse and crystalline As-Te-Ge powder, used above for X-ray diffraction were measured to be -0.38×10^{6} cc/gm and -0.16×10^{6} cc/gm respectively. Both were diamagnetic. Since the crystalline powder contains some amorphouse phase powder, the true susceptibility of the crystalline material can be masked by the diamagnetic contribution from the amorphouse phase. However, this decrease in diamagnetic susceptibility in going from amorphouse phase to the crystalline phase does suggest a decrease in the number of bonded valence electrons.

Now the terminal states of the bistable resistivity As-Te-Ge glass have been determined experimentally. The discussion on the causes of

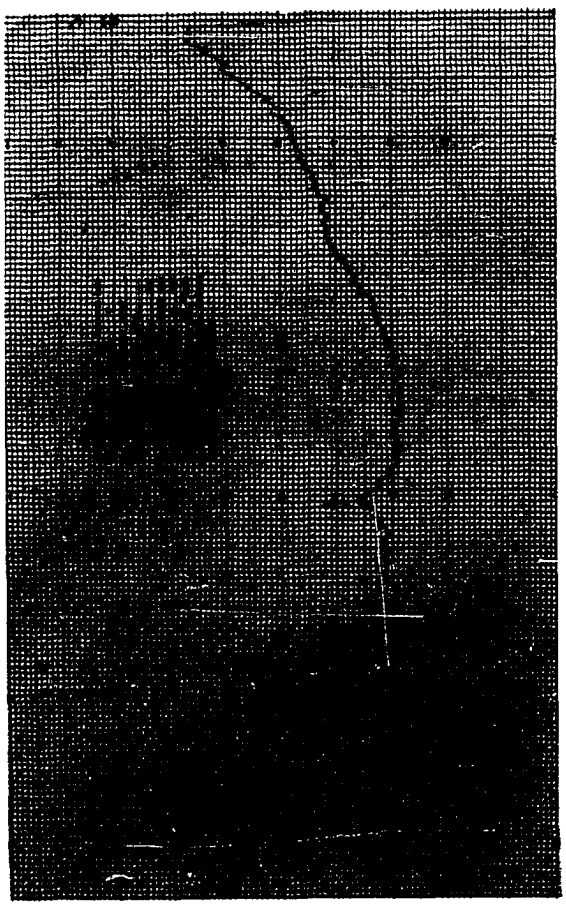


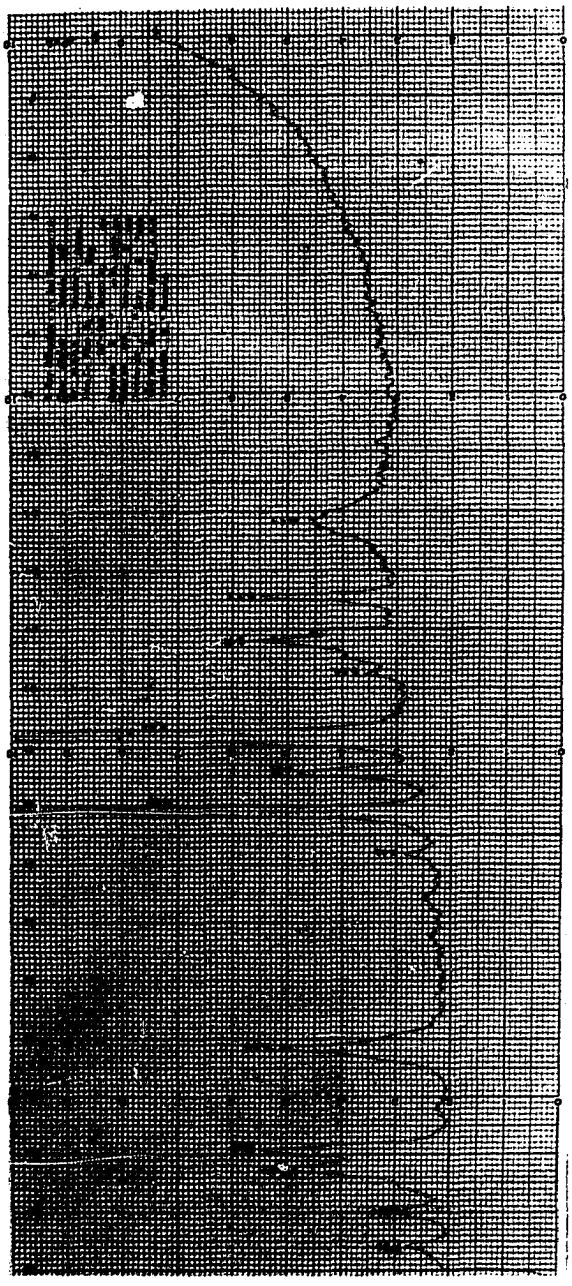
As – Te – Ge (Quenched)

As – Te – Ge (Cooled from 300°c in 4hrs.)

FIGURE 23. 100 x MICROPHOTOGRAPH OF As-Te-Ge BULKS

Figure 24. Powder X-ray diffraction patterns
quenched As-Te-Ge (upper)
As-Te-Ge cooled from 300°C to 25°C in 4 hours (lower)





reversible phase transition will unfortunately be much more speculative than what has transpired so far. No experimental work has been done in supporting the conjectures made here on the causes of phase transitions. At present it is thought that the crystalline to amorphous transition is an electric field induced process while the reverse transition is a joule heating process via the liquid state as sketched in Figure 25. This electronically induced crystallization is not inconceivable since electron beam induced local crystallizations were observed in amorphous CdS film by Schulze (16) and in amorphous Sb film by Levinstein (17). Another example of electronically induced phase transition is the phase transition in the electron compound of copper-zinc alloy (18) induced by a slight variation in average valence electron due to a minute change in composition of the alloy.

The crystalline to amorphous transition can reasonably be assumed to be a transition induced by heating. Contrary to the prevalent belief, this heating process can be a very fast process if the mass involved is small. Ancker-Johnson (19) have measured thermal relaxation time below 1 μs in InSb. Assuming the specific heat of the As-Te-Ge to be 0.065 cal/gm^{o}C which was obtained by averaging according to mass ratio, the temperature rise in a 5000Å thick film in its low resistance state was calculated and plotted in Figure 26 as functions of filament diameter and time interval of the current pulse. It was further assumed in the above calculations that the amplitude of the current pulse was 8 mA and R_1 was 100 ohms and there was no heat loss to the surroundings. The melting point of As-Te-Ge glass is 240^{o}C; therefore, the plot indicated for a

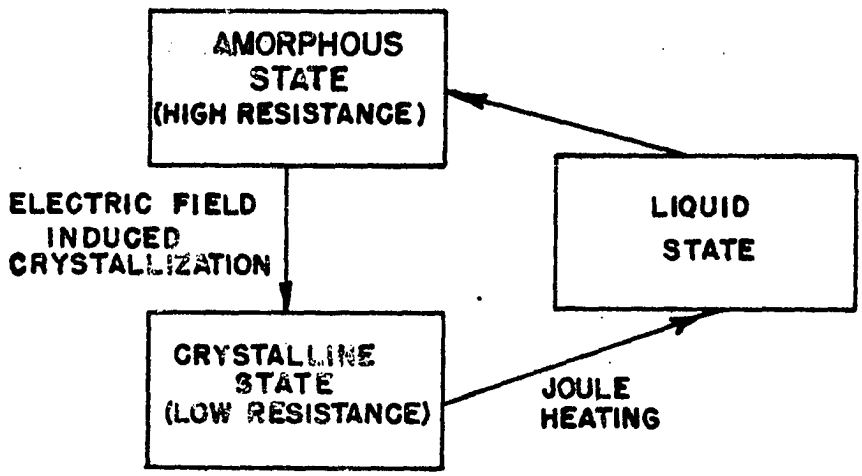


FIGURE 25. STATE TRANSITION DIAGRAM

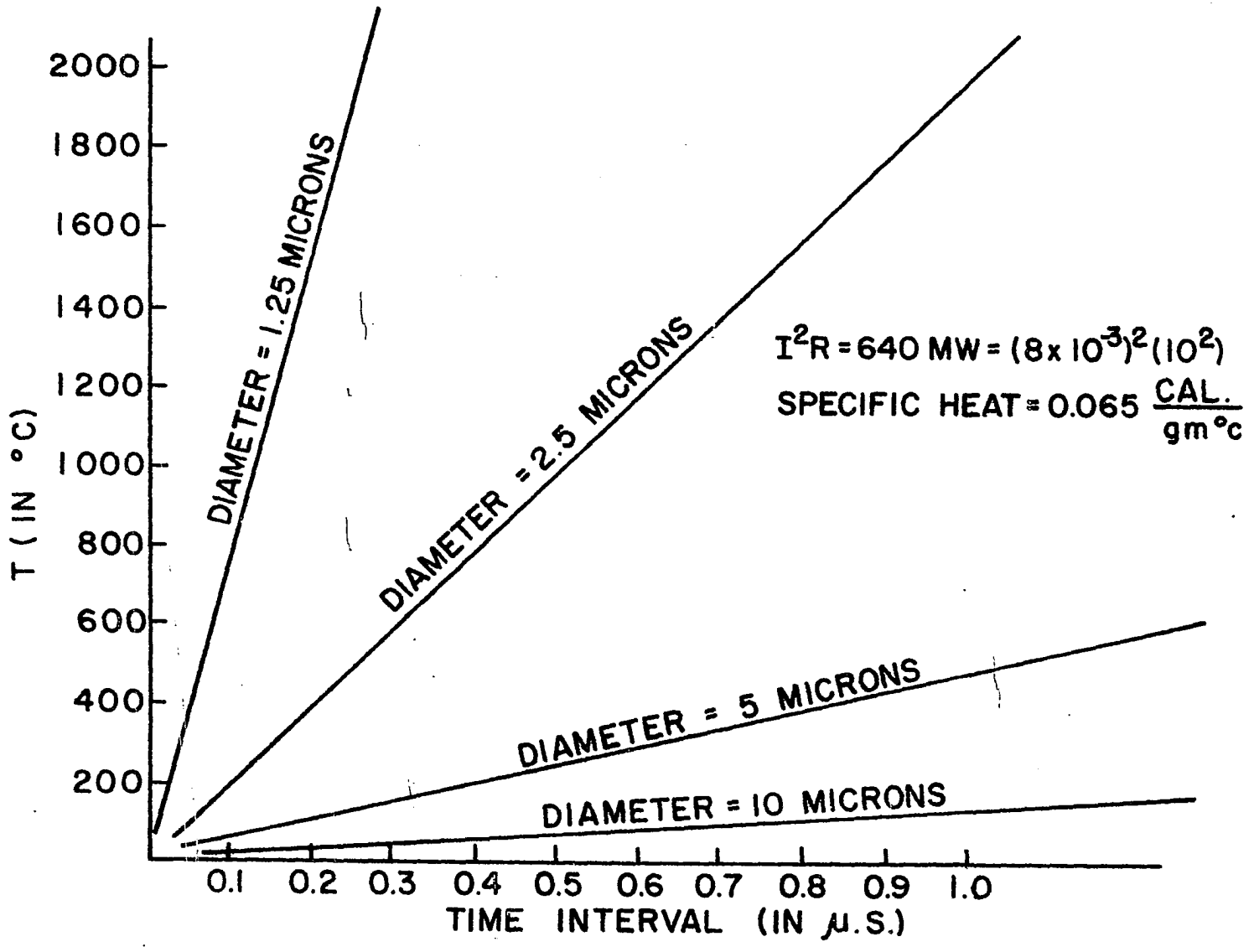


FIGURE 26. TEMPERATURE RISE vs CURRENT TIME INTERVAL

2.5 micron diameter filament a minimum switching time of 0.13 μs is required. This indicated that melting-solidification can be a relatively fast process even with current amplitude below 10 mA. The uncertainty of the above discussion shows that much more work is needed to be done in this area in order to explain the basic nature of this unusual electrically induced phase transition phenomenon.

There is also additional research to be undertaken in order to make this type of BSR glass memory economically feasible and technologically compatible with the silicon integrated circuit process. To make sizable batch fabricated memory array possible, it will be necessary to determine the mechanical properties and the tolerance variation of the electrical properties of evaporated glass film over a reasonably large area. Since in batch fabricated memory array, there is no freedom in selecting the discrete good bit, the uniformity in electrical properties will determine the yield and the realizable array size. One of the electrical properties of the glass film that is most critical for read only memory operation is the stability or the NDRO characteristic of the high and low resistance states under pulsed read operation with read pulse amplitude smaller than the voltage and current threshold values. A reasonable variation in the voltage and current threshold values of the film can be tolerated in this type of slow write and not too often write memory. Because in this type of memory a read cycle can always follow the writing of a word in order to verify the content of the word just written into and correct any error in the word with another write cycle.

Besides hybriding with diode array, the incorporation of BSR glass

with bipolar or IGFET transistor matrix array as sketched in Figure 17 through Figure 21 raises the interesting possibility of non-volatile, high density and low power semiconductor memory. The BSR glass film will be used as the memory element and the active device will serve both as the driver and the sense amplifier for the basic memory cell. The potential usefulness of the BSR in chalcogenide glass definitely warrants further basic and applied research in the area of amorphous semiconductors.

VI. CONCLUSION

The feasibility of using bulk BSR property of chalcogenide glass for sizable electrically alterable read only memory has been established provided a non-linear element such as diode is used in series with the BSR memory element for back coupling isolation. This research has established the following conclusions concerning chalcogenide BSR memory.

1. A chalcogenide glass of As-Te-Ge (55%, 35%, and 10% respectively by atomic percent) does exhibit reproducible bistable resistivity phenomenon. Thin film array of this material can be fabricated by evaporation process.
2. Through equivalent circuit calculation using measured array device parameters, it is established that by using silicon diode for isolation memory module of 10^6 bits with a read cycle time of 200 ns can be built with state of art semiconductor technology, assuming stable electrical and mechanical properties of the glass film, interfaced with the silicon integrated circuit, can be obtained over reasonable area. The projected memory density is 2.5×10^5 bits/in^2.

At present the technology of BSR glass switch is still in its infancy. With further study in the area of this switching mechanism, it is not inconceivable that bistable resistivity glass memory will become feasible for bulk read write memory application.

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VIII. ACKNOWLEDGMENT

I'm deeply grateful to Dr. A. V. Pohm who has patiently guided me into this oasis in the desert of memory research.

I'm also indebted to: Dr. C. Comstock, for indoctrinating me on the fine points of vacuum evaporation; Dr. J. M. Wang, for the wired evaporation mask and the evaporation of aluminum conductor array; Mr. H. Stevenson, for X-ray diffraction patterns and discussions on ceramics; Mr. J. Griener, for the magnetic susceptibility measurements; Mr. F. Laabs, for the electron microprobe analysis; and Miss P. Mohoney, for surface replica electron microscopy.

I'd like to express my appreciation to the Engineering Research Institute of Iowa State University for granting me the research assistantship in the Industrial Affiliate Solid State Electronic Program.

Lastly, I wish to thank my wife, Maureen and my children , Michael, Kathleen and Angela for many personal sacrifices.